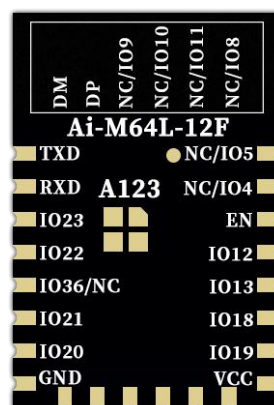
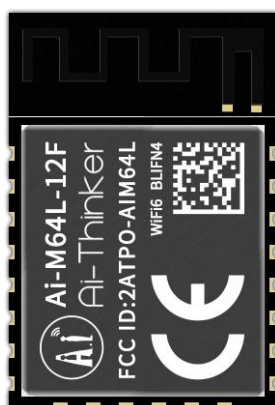


Ai-M64L-12F Specification



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Product Model: Ai-M64L-12F

Version: V1.0.1

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V1.0.0	2026-06-23	First edition	Wang Yeqing	Guan Ning
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1 Product Overview

The Ai-M64L-12F is a standardized wireless module based on the Bouffalo Lab BL616CL RF chip, designed specifically for ultra-low-power, high-performance, and high-security IoT scenarios. Fully retaining the chip-level RF performance and full-function peripherals, the module undergoes rigorous RF matching and reliability verification with plug-and-play capability, significantly reducing the development barriers and mass-production risks of end products. The product features five core features: strong signal performance, low power consumption, high integration, security and reliability, and ultra-compact package, while also supporting backward compatibility with modules of the same type.

Figure 1 shows the BL616CL main chip architecture.

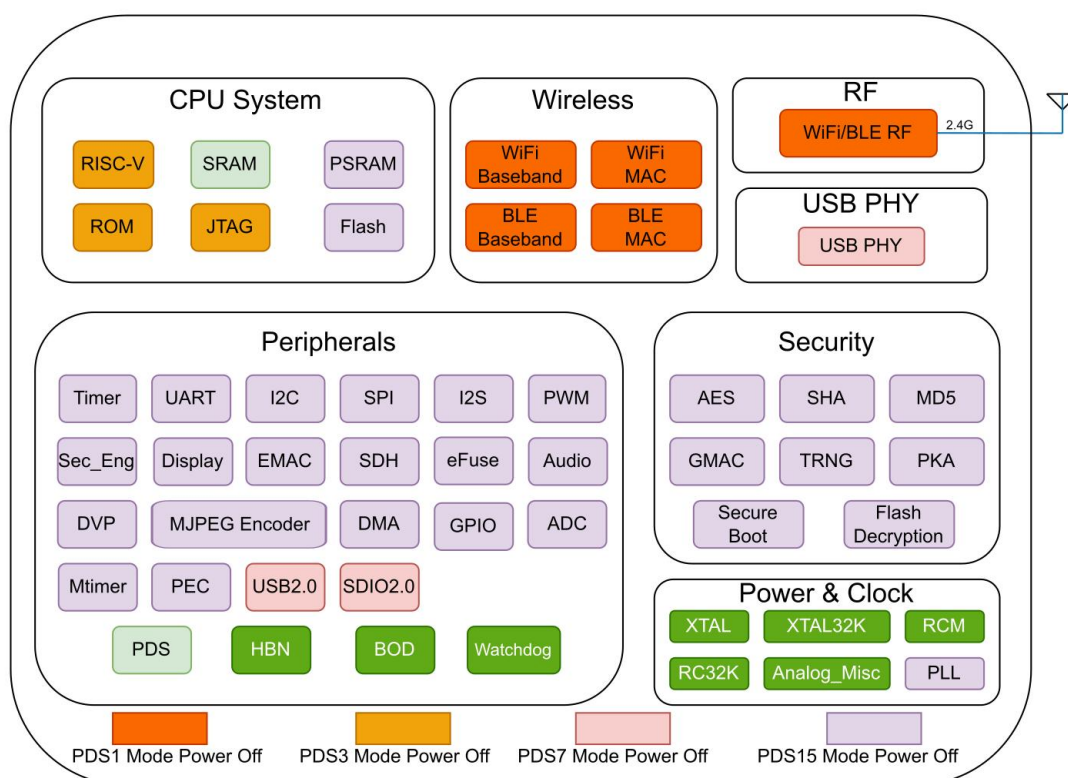


Figure 1 Main Chip Architecture Diagram

1.1 Features

Wireless

- 2.4 GHz RF transceiver
- Wi-Fi 6 (IEEE 802.11b/g/n/ax), 20MHz bandwidth, 1T1R
- Bluetooth® 5.3, multi-rate: 2Mbps/1Mbps/500kbps/125kbps
- Wi-Fi/BLE coexistence, supports BLE-assisted Wi-Fi fast connection
- Supports LDPC, STBC, Beamformee, DL/UL OFDMA, MU-MIMO, TWT (Target Wake Time), SR (Spatial Reuse), DCM (Dual Carrier Modulation), ER (Extended Range)
- Supports aggregation (AMPDU, AMSDU), immediate block ACK, fragmentation and defragmentation
- Supports RX diversity
- Supports IEEE 802.11e QoS WMM (Wi-Fi Multimedia), IEEE 802.11w PMF (Protected Management Frames)
- STA, SoftAP, STA+SoftAP, and sniffer modes
- Integrated RF balun, PA/LNA, supports external PA/LNA

Microcontroller Subsystem

- 32-bit RISC-V CPU, supports RISC-V RV32IMAFCP instruction set
- Dynamic frequency from 1MHz to 320MHz
- Integrated FPU

Memory

- 388KB SRAM
- 224KB OCRAM
- 160KB WRAM
- 4KB HBN RAM
- BL616CL chip embedded with 2/4/8MB Flash (optional)
- Supports external Flash expansion (customized)

Security

- Secure boot (supports firmware encryption & signing)
- Supports Anti-Rollback
- XIP On-The-Fly AES Decryption (OTFAD)
- Supports TrustZone
- AES-ECB/CBC/CTR/GMAC/XTS modes
- MD5, SHA-1/224/256/384/512
- TRNG (True Random Number Generator)
- PKA (Public Key Accelerator) for RSA/ECC
- Total 1024 bits eFuse

Peripherals

- USB, UART, I2C, SPI, PWM, GPTimer, Watchdog, ADC, etc.

Development Environment

- Supports secondary development, integrated with Windows and Linux development environments

Power Characteristics

- Receive current: 70mA
- Transmit current: 802.11ax, MCS9, POUT=+17dBm: 276.75mA (average)
- PDS power consumption, DTIM10: 194.46μA
- HBN power consumption: 6.42μA

Physical Characteristics

- Package: SMD-22
- Module dimensions (L × W × H): 24.00 × 16.00 × 3.10mm
- Antenna type: onboard antenna
- Operating temperature: -40 – 85°C
- Storage environment: -40 – 125°C, < 90% RH

Electrical Characteristics

- Supply voltage: 2.97 – 3.63V (typical value 3.3V)
- Supply current: > 500mA
- Communication interface: standard UART interface
- Available I/Os: 19 GPIOs by default
- Protection: built-in ESD protection circuit

Note: For features not marked, please refer to the official BL616CL chip datasheet.

1.2 Application Scenarios

- Audio/Video Multimedia
- Internet of Things (IoT)
- Mobile Devices
- Smart Home
- Control Equipment

2 Key Specifications

Table 1 summarizes the key electrical and physical parameters of the Ai-M64L-12F module.

Table 1 Key Specifications

Model	Ai-M64L-12F
Package	SMD-22
Dimensions	24.00 × 16.00 × 3.10mm
Antenna Type	Onboard antenna
Frequency Range	2400 – 2483.5MHz
Operating Temperature	-40 – 85°C
Storage Conditions	-40 – 125°C, <90% RH
Power Supply Range	Supply voltage: 2.97 – 3.63V, typical 3.3V; supply current > 500mA
Available I/Os	19 by default
UART Rate	115200bps by default
Security	WPS/WEP/WPA/WPA2/WPA3
Flash	4MByte by default, supports up to 16MByte

3 Electrical Characteristics

3.1 Recommended Operating Conditions

Table 2 lists the recommended operating electrical parameters of the Ai-M64L-12F module. Operating outside these ranges may cause device damage.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Supply Voltage	2.97	3.3	3.63	V
I	Supply Current	500	-	-	mA

3.2 I/O DC Electrical Characteristics

Table 3 lists the I/O DC characteristics of the Ai-M64L-12F module. These parameters are mainly used for external interface level matching and GPIO circuit design.

Table 3 I/O DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VIH	High-level Input Voltage	2	-	-	
VIL	Low-level Input Voltage	-	-	0.8	V
VOH	High-level Output Voltage	-	$0.9 \times VCC$	-	V
VOL	Low-level Output Voltage	-	$0.1 \times VCC$	-	V

3.3 Electrostatic Discharge

Figure 2 shows the ESD protection diagram. Ai-M64L-12F is an ESD-sensitive device and requires special precautions during handling.



Figure 2 ESD Protection Diagram

3.4 Wi-Fi RF Performance

Table 4 lists the Wi-Fi performance parameters of the Ai-M64L-12F module. The RF performance parameters are measured under typical test conditions. Actual performance may be affected by the antenna, power supply, PCB layout, test environment, and other factors.

Table 4 Wi-Fi RF Performance

Description	Typ			Unit
Frequency Range	2400 – 2483.5			MHz
Output Power				
Mode	Min	Typ	Max	Unit
802.11b, 11Mbps	-	19	-	dBm
802.11g, 54Mbps	-	18	-	dBm
802.11n, HT20 (MCS7)	-	18	-	dBm
802.11ax, HE20 (MCS9)	-	15	-	dBm
Receiver Sensitivity				
Mode	Min	Typ	Max	Unit
802.11b, 1Mbps	-99	-	-	dBm
802.11b, 11Mbps	-90	-	-	dBm
802.11g, 6Mbps	-93	-	-	dBm
802.11g, 54Mbps	-78	-	-	dBm
802.11n, HT20 (MCS7)	-75	-	-	dBm
802.11ax, HE20 (MCS9)	-67	-	-	dBm

3.5 BLE RF Performance

Table 5 lists the BLE performance parameters of the Ai-M64L-12F module. The RF performance parameters are measured under typical test conditions. Actual performance may be affected by the antenna, power supply, PCB layout, test environment, and other factors.

Table 5 BLE RF Performance

Description	Typ			Unit
Frequency Range	2400 – 2483.5			MHz
Output Power				
Rate Mode	Min	Typ	Max	Unit
1Mbps	-	10	15	dBm
2Mbps	-	10	15	dBm
Receiver Sensitivity				
Rate Mode	Min	Typ	Max	Unit
1Mbps sensitivity@30.8% PER	-97	-	-	dBm
2Mbps sensitivity@30.8% PER	-95	-	-	dBm

3.6 Power Consumption

Table 6 lists the power consumption data of the Ai-M64L-12F module in different modes. The following power consumption data are measured under a 3.3V power supply and 25°C ambient temperature.

- The P_{OUT} power for all transmit modes is measured at the antenna interface.
- All transmission data are measured at 100% duty cycle in continuous transmit mode.

Table 6 Power Consumption

Mode	Min	Avg	Max	Unit
TX 802.11b, 11Mbps, $P_{OUT} = +23\text{dBm}$	-	410.52	-	mA
TX 802.11g, 54Mbps, $P_{OUT} = +20\text{dBm}$	-	337.71	-	mA
TX 802.11n, MCS7, $P_{OUT} = +19\text{dBm}$	-	322.60	-	mA
TX 802.11ax, MCS9, $P_{OUT} = +17\text{dBm}$	-	276.75	-	mA
RX 802.11b, Packet Length 1500 bytes	-	70.60	-	mA
RX 802.11g, Packet Length 1500 bytes	-	70.67	-	mA
RX 802.11n, Packet Length 1500 bytes	-	69.07	-	mA
RX 802.11ax, Packet Length 1500 bytes	-	69.82	-	mA
PDS Power Consumption, DTIM Level 10	-	194.46	-	μA
HBN Power Consumption	-	6.42	-	μA

4 Mechanical Specifications

4.1 Module Dimensions

Figure 3 shows the outline dimensions of the Ai-M64L-12F module. The outline dimensions ($L \times W \times H$) are $24.00 \times 16.00 \times 3.10\text{mm}$. The dimensional tolerance is $\pm 0.20\text{mm}$.

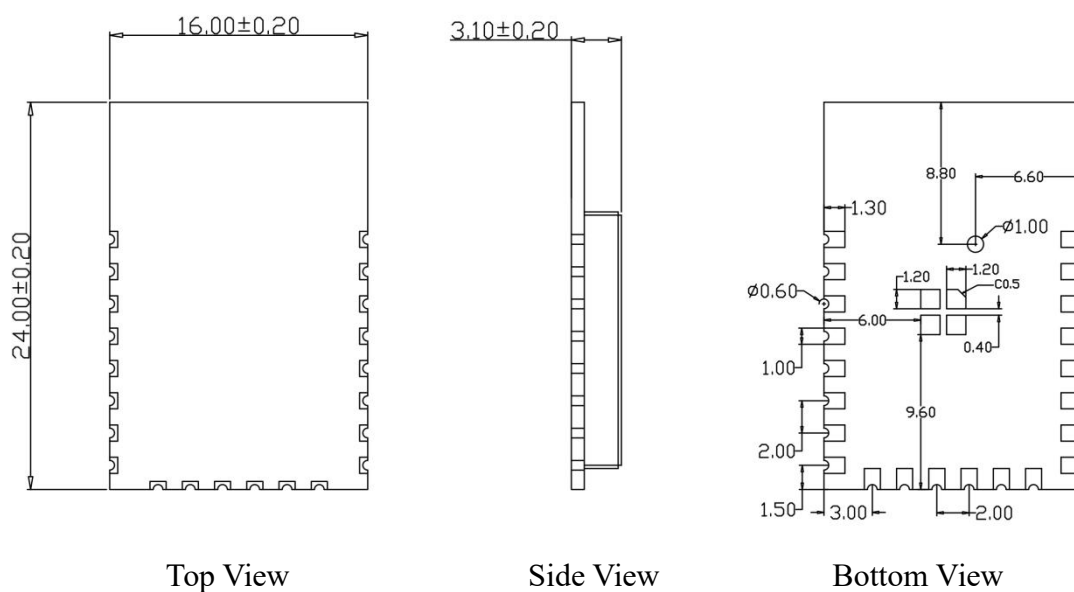


Figure 3 Module Dimensions (Unit: mm)

4.2 Shield Cover Marking Information

Figure 4 shows the shield cover marking information of the Ai-M64L-12F module. Each character corresponds to module configuration information such as chip brand, Flash size, and temperature version.

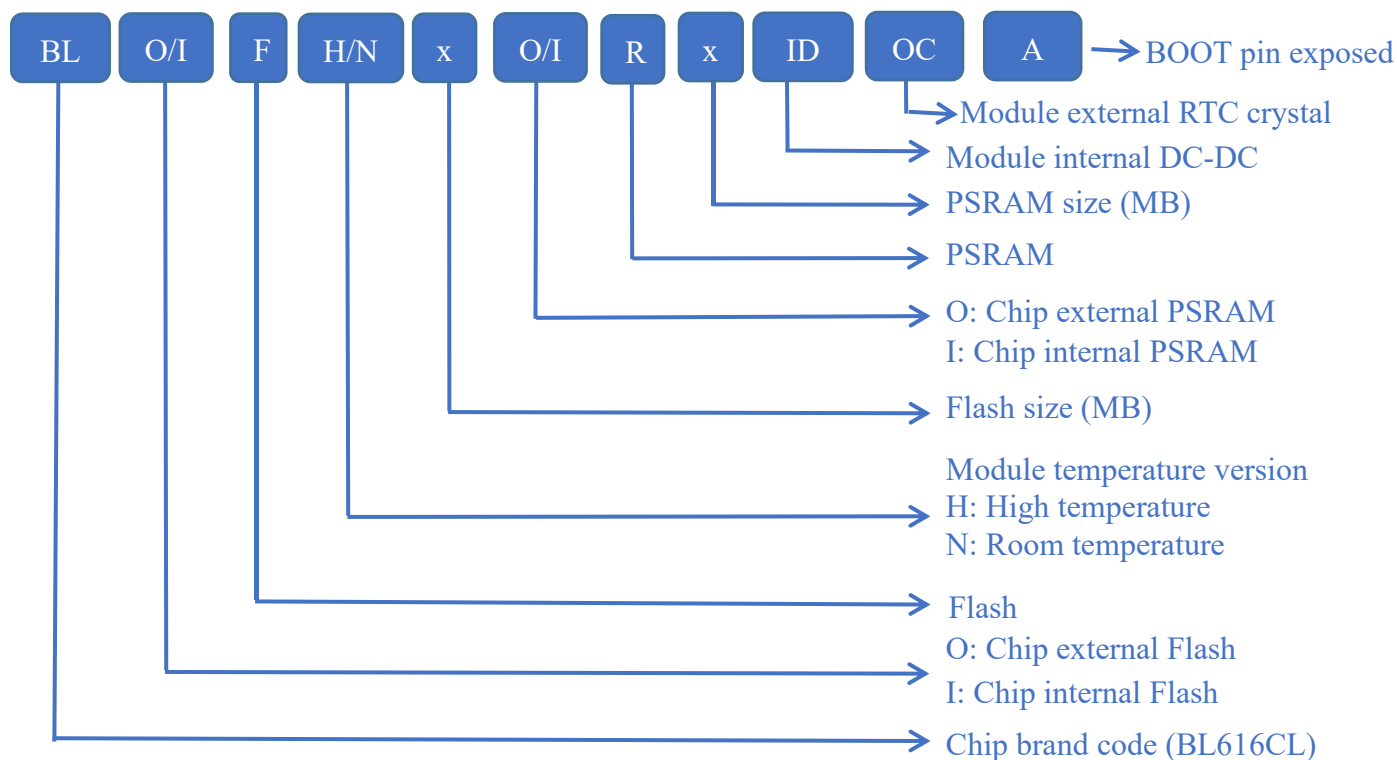


Figure 4 Shield Cover Marking Information

5 Pin Definition

Figure 5 shows the top and bottom views of the Ai-M64L-12F module's pin layout, with a total of 22 pins exposed.

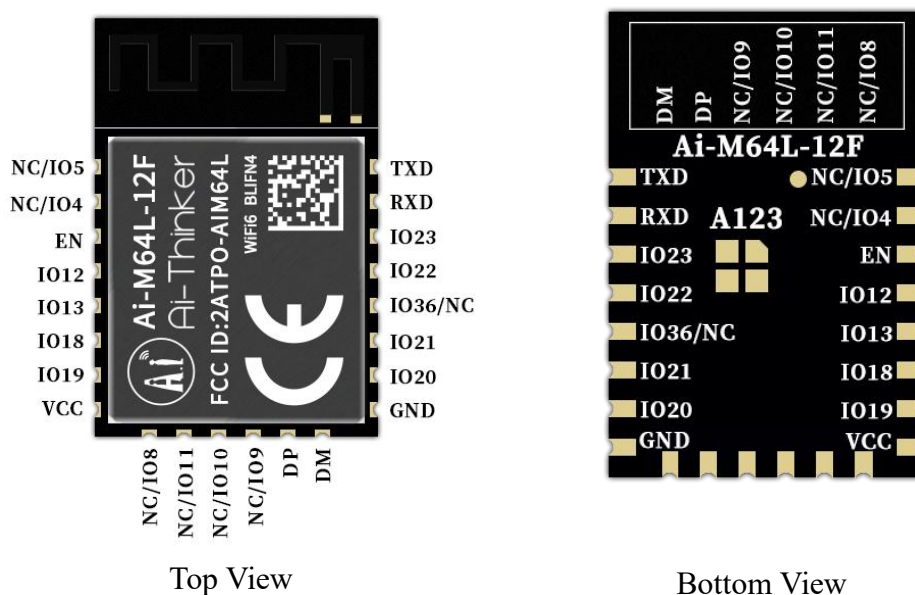


Figure 5 Pin Diagram

Table 7 defines the pin functions of the Ai-M64L-12F module, including pin number, pin name, and function description.

Table 7 Pin Function Definition

No.	Name	Function
1	NC/IO5	GPIO5/SPI0_SCLK/SPI1_SCLK/I2S_FS/I2C_SDA/UART_SIG5/ADC_CH5/PWM0_CH1P/PWM0_CH2N/DBI_TypeC_DCn/JTAG_TCK (Available by default. This IO shares the internal 32.768kHz crystal output pin. For modules with built-in RTC crystal, this IO is NC.)
2	NC/IO4	GPIO4/SPI0_SS/SPI1_SS/I2S_BCLK/I2C_SCL/UART_SIG4/ADC_CH4/PWM0_CH0P/PWM0_CH2P/DBI_TypeC_SDA/JTAG_TMS (Available by default. This IO shares the internal 32.768kHz crystal input pin. For modules with built-in RTC crystal, this IO is NC.)
3	EN	Chip enable by default, active high
4	IO12	GPIO12/SPI0_SS/SPI1_SS/I2S_BCLK/I2C_SCL/UART_SIG0/RMII_MDIO/CAM_DAT0/ADC_CH8/PWM0_CH0P/PWM0_CH2P/DBI_TypeB_DB0/DBI_TypeC_SDA/DISP_QSPI_SCL/AUPWM_P/JTAG_TMS
5	IO13	GPIO13/SPI0_SCLK/SPI1_SCLK/I2S_FS/I2C_SDA/UART_SIG1/RMII_MDC/CAM_DAT1/ADC_CH9/PWM0_CH1P/PWM0_CH2N/DBI_TypeB_DB1/DBI_TypeC_DCn/DISP_QSPI_CSn/AUPWM_N/JTAG_TCK

6	IO18	GPIO18/SPI0_MISO/SPI1_MISO/I2S_DI/I2S_RCLK_O/I2C_SCL/UART_SIG6/RMII_RXD[1]/CAM_DAT6/PWM0_CH2P/PWM0_CH1P/DBI_TypeB_DB6/DBI_TypeC_SCL/DISP_QSPI_SCL/AUPWM_P/JTAG_TDO
7	IO19	GPIO19/SPI0_MOSI/SPI1_MOSI/I2S_DO/I2S_RCLK_O/I2C_SDA/UART_SIG7/RMII_RXD[0]/CAM_DAT7/PWM0_CH3P/PWM0_CH1N/DBI_TypeB_DB7/DBI_TypeC_CSn/DISP_QSPI_CSn/AUPWM_N/JTAG_TDI
8	VCC	3.3V power supply, current recommended to be above 500mA.
9	NC/IO8	GPIO8/SPI0_SS/SPI1_SS/I2S_BCLK/I2C_SCL/UART_SIG8/SF2_D2/SDIO_CMD/PWM0_CH0P/DBI_TypeC_SDA/DISP_QSPI_SDA0/JTAG_TMS (Available by default. This IO shares the internal Flash pin. For modules with external Flash, this IO is NC.)
10	NC/IO11	GPIO11/SPI0_MOSI/SPI1_MOSI/I2S_DO/I2S_RCLK_O/I2C_SDA/UART_SIG11/SF2_D3/SDIO_DAT1/PWM0_CH3P/PWM0_CH1N/DBI_TypeC_CSn/DISP_QSPI_SDA3/JTAG_TDI (Available by default. This IO shares the internal Flash pin. For modules with external Flash, this IO is NC.)
11	NC/IO10	GPIO10/SPI0_MISO/SPI1_MISO/I2S_DI/I2S_RCLK_O/I2C_SCL/UART_SIG10/SF2_CLK/SDIO_DAT0/PWM0_CH2P/PWM0_CH1P/DBI_TypeC_SCL/DISP_QSPI_SDA2/JTAG_TDO (Available by default. This IO shares the internal Flash pin. For modules with external Flash, this IO is NC.)
12	NC/IO9	GPIO9/SPI0_SCLK/SPI1_SCLK/I2S_FS/I2C_SDA/UART_SIG9/SF2_D0/SDIO_CLK/PWM0_CH1P/PWM0_CH0N/DBI_TypeC_DCn/DISP_QSPI_SDA1/JTAG_TCK (Available by default. This IO shares the internal Flash pin. For modules with external Flash, this IO is NC.)
13	DP	USB_DP/GPIO32/SPI0_SS/SPI1_SS/I2S_BCLK/I2C_SCL/UART_SIG8/PDM_CLK/ADC_CH10/PWM0_CH0P/DBI_TypeC_SDA/JTAG_TMS
14	DM	USB_DM/GPIO33/SPI0_SCLK/SPI1_SCLK/I2S_FS/I2C_SDA/UART_SIG9/PDM_IN/ADC_CH11/PWM0_CH1P/PWM0_CH0N/DBI_TypeC_DCn/JTAG_TCK
15	GND	Ground
16	IO20	GPIO20/SPI0_SS/SPI1_SS/I2S_BCLK/I2C_SCL/UART_SIG8/PDM_CLK/RMII_RX_DV/CAM_VSYNC/PWM0_CH0P/PWM0_CH2P/DBI_TypeC_SDA/DISP_QSPI_SDA0/JTAG_TMS
17	IO21	GPIO21/SPI0_SCLK/SPI1_SCLK/I2S_FS/I2C_SDA/UART_SIG9/PDM_IN/CAM_CLK/PWM0_CH1P/PWM0_CH2N/DBI_TypeC_DCn/DISP_QSPI_SDA1/JTAG_TCK
18	IO36/NC	GPIO36/SPI0_SS/SPI1_SS/I2S_BCLK/I2C_SCL/UART_SIG0/PWM0_CH0P/PWM0_CH2P/DBI_TypeB_DCn/JTAG_TMS/Bootstrap (For module versions with marking suffix “A”, this pin is exposed to the

		edge castellated pad. For modules without the “A” suffix, this pin is NC.)
19	IO22	GPIO22/SPI0_MISO/SPI1_MISO/I2S_DI/I2S_RCLK_O/I2C_SCL/UART_SIG10/CAM_HSYNC/PWM0_CH2P/PWM0_CH3P/DBI_TypeC_SCL/DISP_QSPI_SDA2/JTAG_TDO
20	IO23	GPIO23/SPI0_MOSI/SPI1_MOSI/I2S_DO/I2S_RCLK_O/I2C_SDA/UART_SIG11/RMII_MDIO/CAM_VSYNC/SWGPIO[23]/PWM0_CH3P/PWM0_CH3N/DBI_TypeC_CSn/DISP_QSPI_SDA3/JTAG_TDI
21	RXD	GPIO35/SPI0_MOSI/SPI1_MOSI/I2S_DO/I2S_RCLK_O/I2C_SDA/UART_SIG11/PWM0_CH3P/PWM0_CH1N/DBI_TypeC_CSn/JTAG_TDI
22	TXD	GPIO34/SPI0_MISO/SPI1_MISO/I2S_DI/I2S_RCLK_O/I2C_SCL/UART_SIG10/PWM0_CH2P/PWM0_CH1P/DBI_TypeC_SCL/JTAG_TDO
Note: Both IO36 and the test point on the back of the module can be used as Bootstrap. When the voltage is high at power-up, the module enters flashing mode; when the voltage is low at power-up, the module boots normally. The module internal default is low level.		

6 Schematic

Figure 6 shows the schematic of the Ai-M64L-12F module, integrating RF antenna, power supply, clock, and reserved peripheral interfaces.

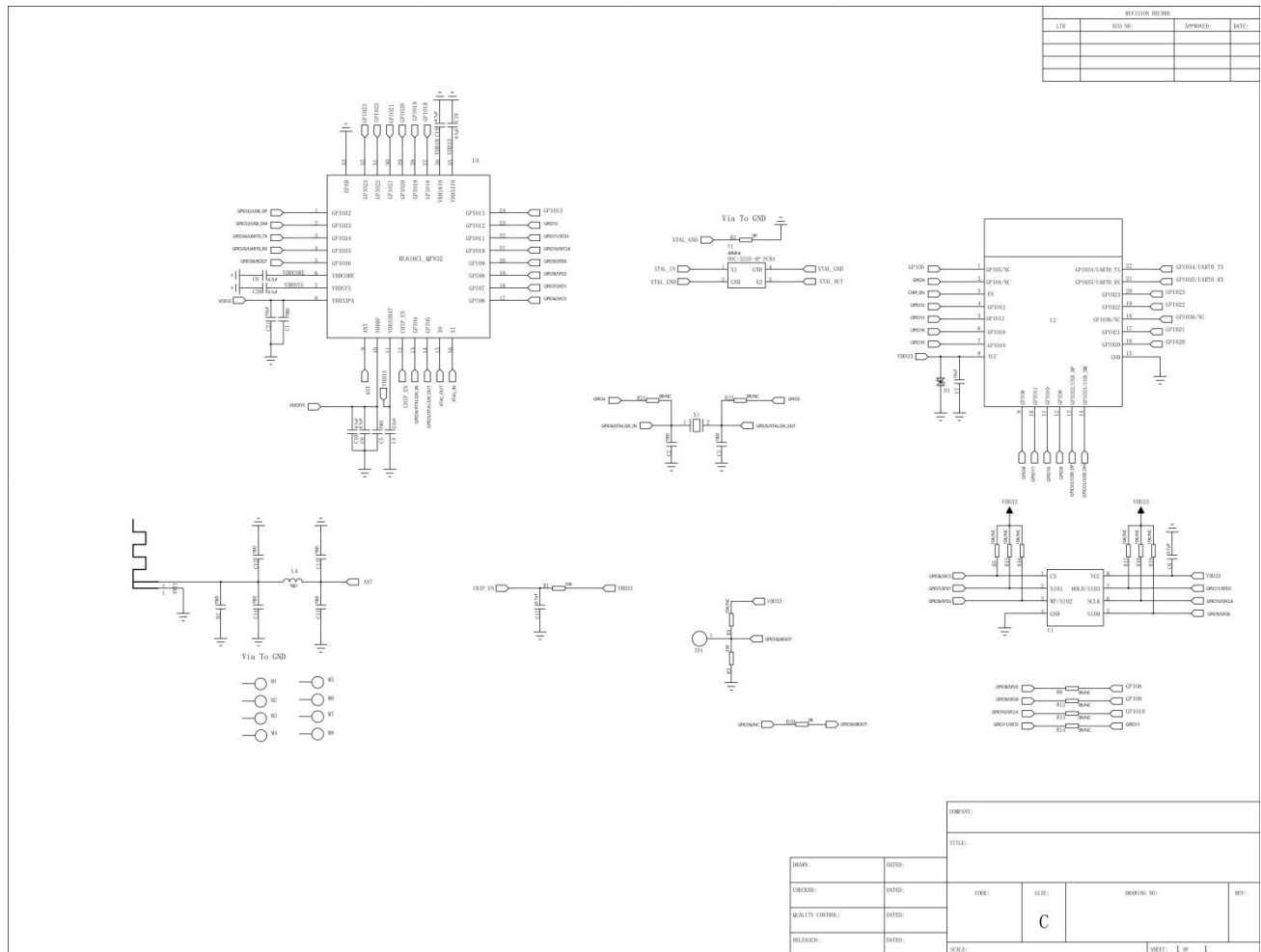


Figure 6 Schematic

7 Antenna Parameters

7.1 Antenna Test Prototype

Figure 7 shows the antenna test prototype of the Ai-M64L-12F module. The green test board carries the wireless module, with RF and power signal lines routed out for RF testing.

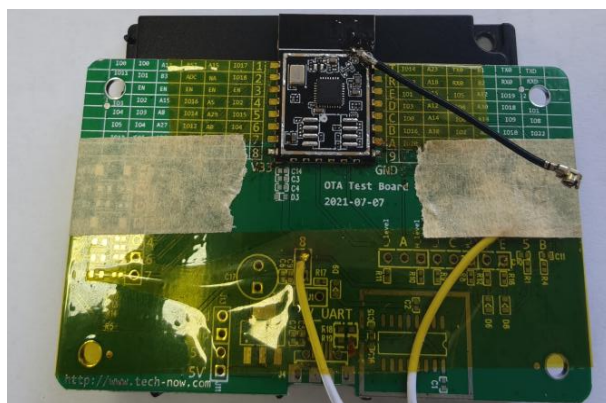


Figure 7 Antenna Test Prototype

7.2 Antenna S-Parameters

Figure 8 shows the antenna S-parameter results of the Ai-M64L-12F module measured by a network analyzer, including three RF characteristic curves: Smith chart, S11 return loss and VSWR.

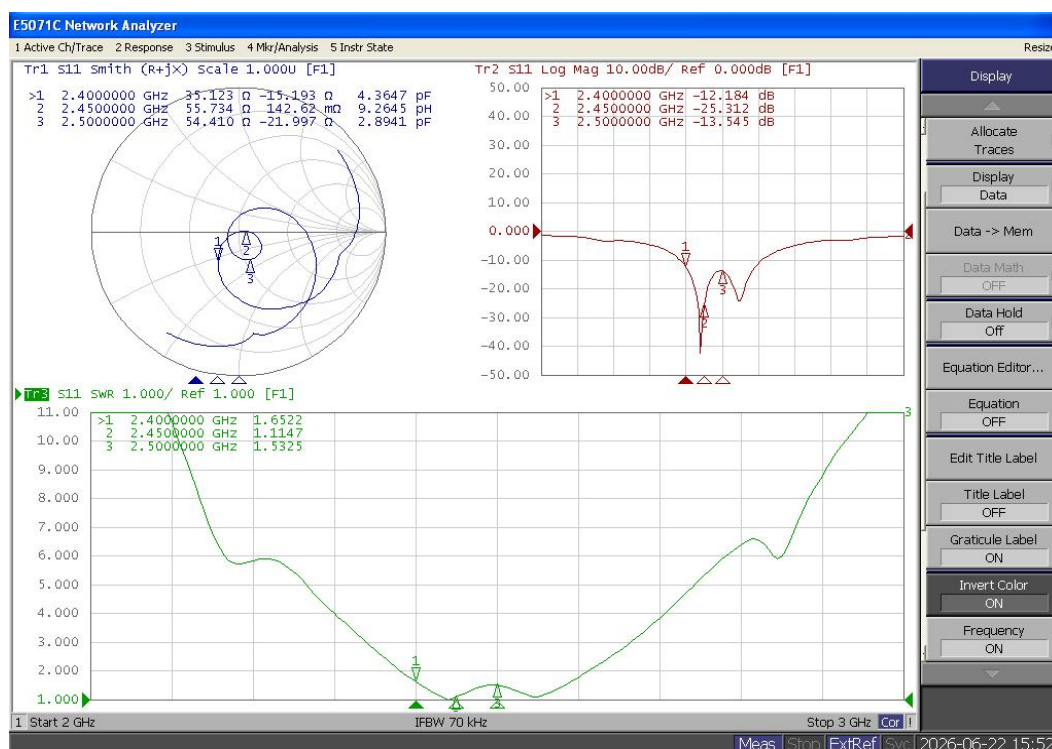


Figure 8 Antenna S-Parameters

7.3 Antenna Gain and Efficiency

Table 8 shows the measured gain and radiation efficiency parameters of the Ai-M64L-12F module's antenna at each frequency point within the 2400 – 2500MHz operating band.

Table 8 Antenna Gain and Efficiency

No.	1	2	3	4	5	6	7	8	9	10	11
Frequency (MHz)	2400	2410	2420	2430	2440	2450	2460	2470	2480	2490	2500
Gain (dBi)	1.31	1.55	1.77	1.82	1.43	1.41	1.12	1.08	1.22	1.26	1.22
Efficiency (%)	44.44	45.93	46.35	47.21	44.32	44.02	43.20	43.74	43.16	40.99	43.67

7.4 Antenna Radiation Pattern

Figure 9 shows the 3D radiation pattern and planar cut patterns of the Ai-M64L-12F module's antenna at a typical 2.4GHz frequency point.

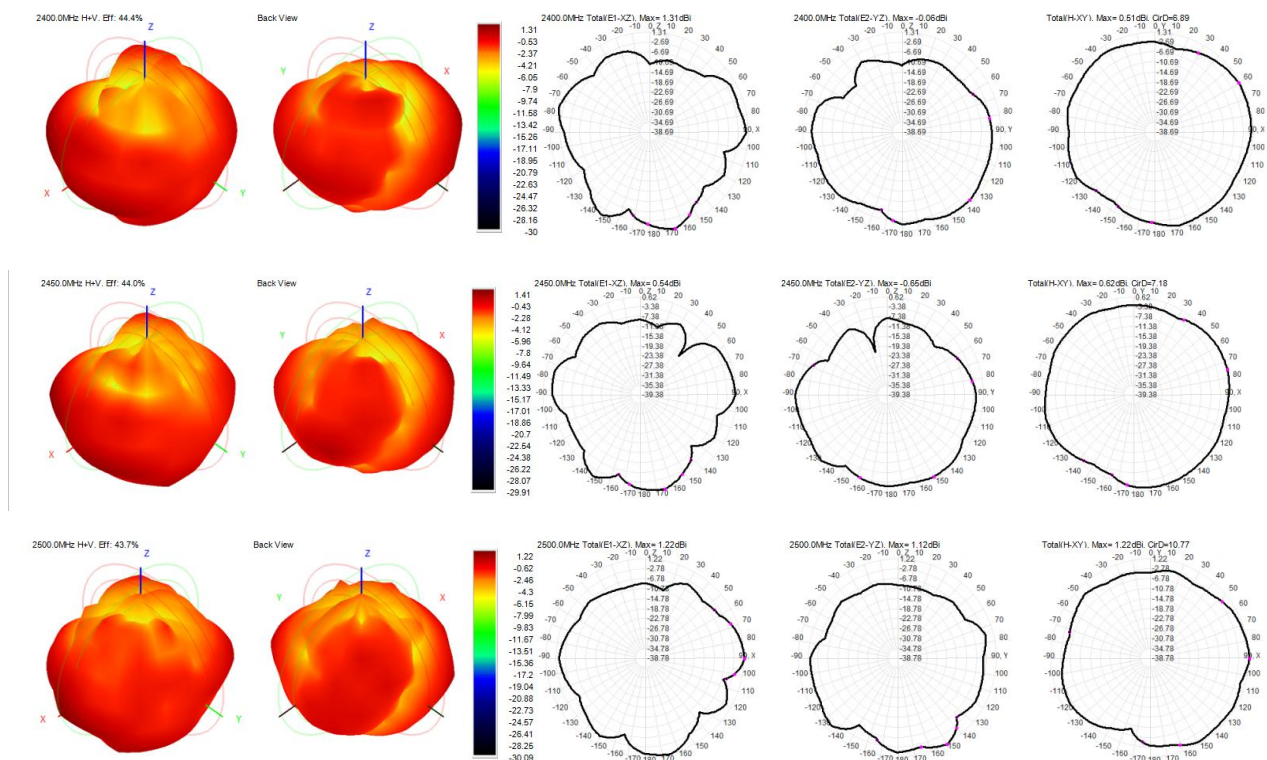


Figure 9 Antenna Radiation Pattern

8 Design Guide

8.1 Application Reference Circuit

Figure 10 shows the hardware application reference circuit for the Ai-M64L-12F module, illustrating the serial communication, power supply, enable, and program download interface connections.

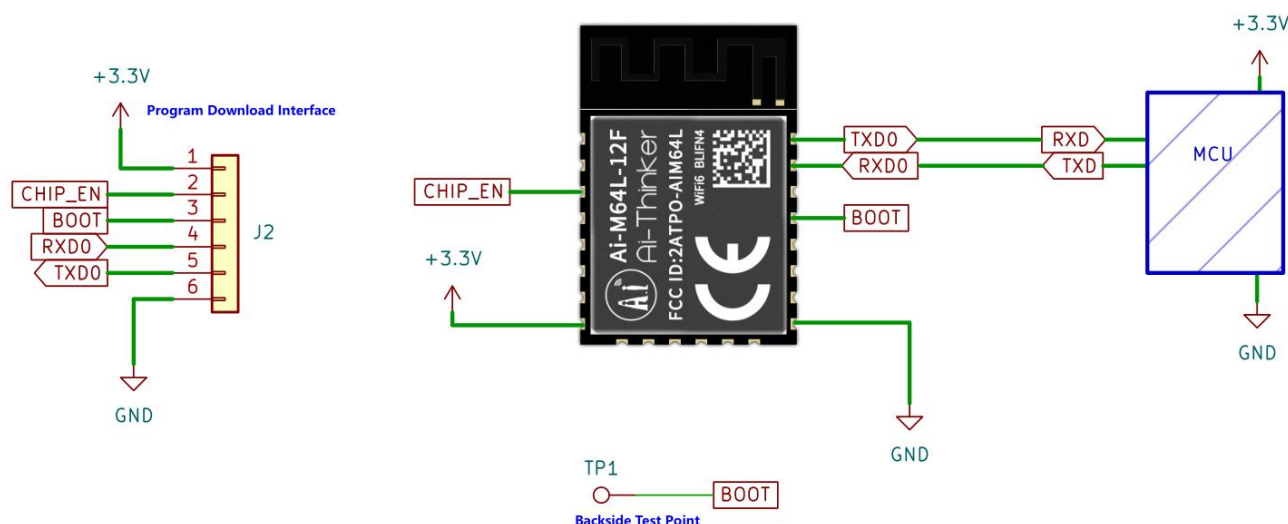


Figure 10 Application Reference Circuit

Notes on the Application Reference Circuit:

- VCC supply voltage: 2.97 – 3.63V. The external power supply output current is recommended to be above 500mA.
- The Boot pin for all modules in this series is located on the test point on the back of the module. For module versions with marking suffix “A”, the chip’s Boot configuration pin is exposed to the edge castellated pad, corresponding to module pin IO36. Module versions without the “A” suffix do not have this pin exposed.
- For module versions with marking suffix “A”, both IO36 (castellated pad) and the back test point pad can be used as the download Boot pin. It is recommended to prioritize IO36 (castellated pad) as the download interface configuration pin, and it is not recommended to use this IO as a regular GPIO. If this IO must be used, the external circuit’s power-on startup timing must meet the timing requirements of the Boot pin.

8.2 Recommended PCB Footprint Dimensions

Figure 11 shows the recommended PCB footprint dimensions of the Ai-M64L-12F module. The pad dimensions (L × W) are 1.80 × 1.00mm. The center-to-center spacing between adjacent pads is 2.00mm.

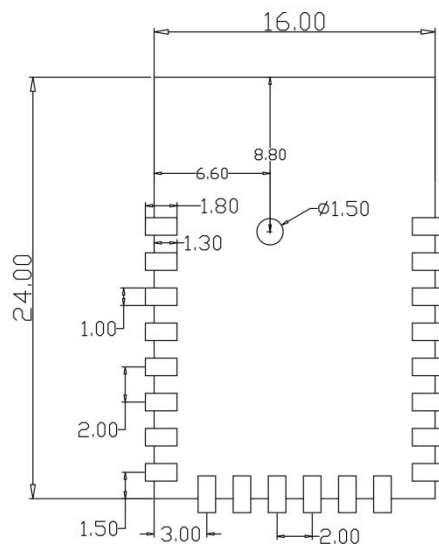


Figure 11 Recommended PCB Footprint Dimensions (Unit: mm)

8.3 Power Supply

Figure 12 shows a DC-DC buck power supply circuit converting 12V to 3.3V, with a maximum output current of 2A.

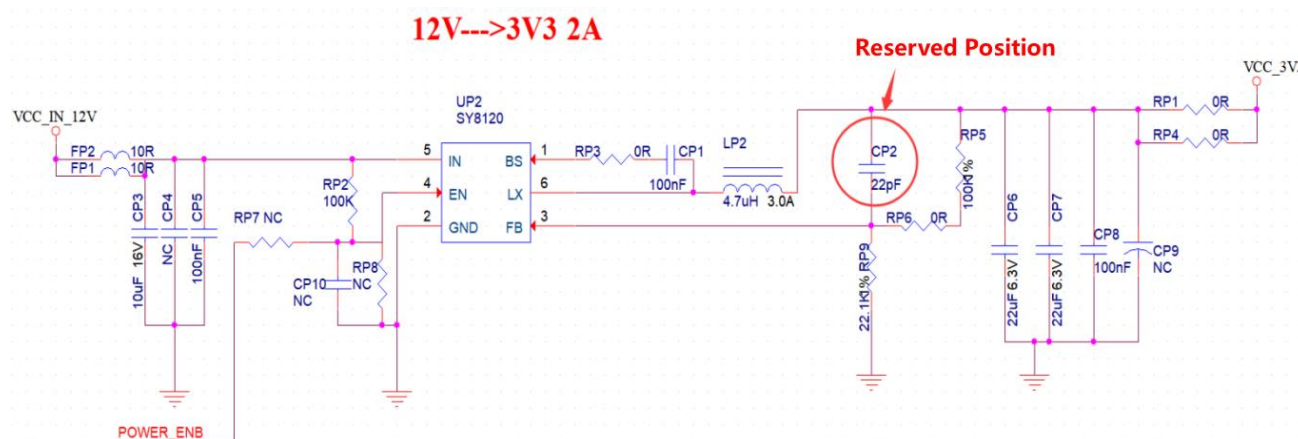


Figure 12 DC-DC Buck Circuit

Notes on the DC-DC Buck Circuit:

- VDD is recommended as 3.3V, with a peak current above 500mA.
- An LDO is recommended for power supply; if using DC-DC, the ripple should be controlled within 30mV.
- For the DC-DC power supply circuit, it is recommended to reserve space for dynamic response capacitors to optimize output ripple under large load transients.
- It is recommended to add ESD protection devices to the power interface.

8.4 GPIO

Figure 13 shows a 3.3V and 5V bidirectional UART level-shifting circuit, which supports bidirectional serial communication across different voltage levels.

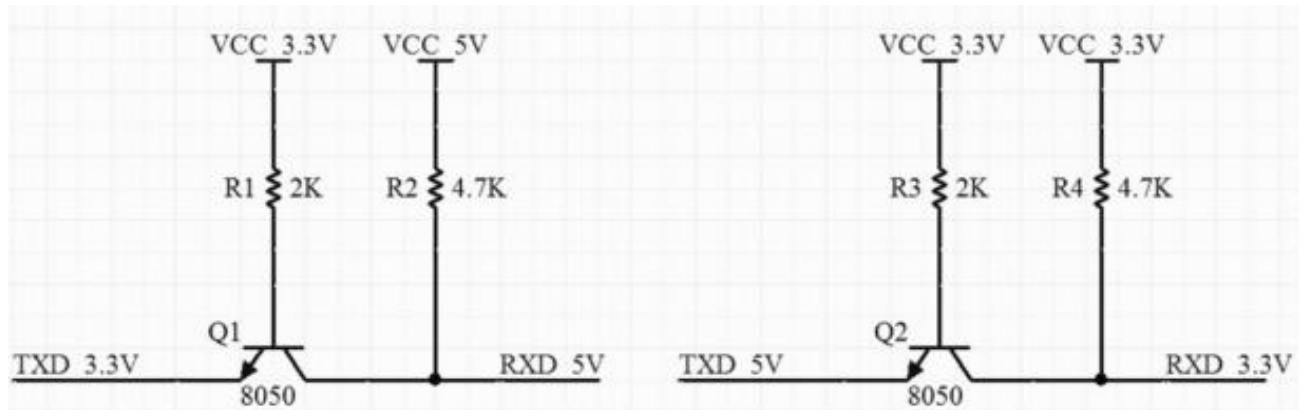


Figure 13 Level-shifting Circuit

Notes on the Level-Shifting Circuit:

- Some I/O pins are brought out from the module. To use these I/O pins, it is recommended to connect a 10-100Ω resistor in series with each I/O pin. This helps suppress overshoot, stabilize signal levels, and benefits both EMI and ESD protection.
- The pull-up or pull-down configuration for special I/O pins must refer to the instructions in the specification, as it affects the module boot configuration.
- The module I/O pins level is 3.3V. If the host controller I/O voltage level does not match the module, a level-shifting circuit should be added.
- If an I/O pin is directly connected to a peripheral interface or pin headers, it is recommended to reserve space for an ESD protection device near the connector on the I/O trace.

9 Storage Conditions

Products sealed in moisture barrier bags should be stored in a non-condensing atmosphere at $< 40^{\circ}\text{C}$ and $< 90\% \text{ RH}$.

The moisture sensitivity level (MSL) of the module is level 3.

The module must be used within 168 hours after vacuum bag removal under conditions of $25\pm 5^{\circ}\text{C}$ and 60% RH. Otherwise, the module requires baking before being returned to production.

10 Reflow Soldering Profile

Figure 14 shows the module reflow soldering process profile. The process is divided into four stages: ramp-up zone, preheat/soak zone, reflow soldering zone and cooling zone.

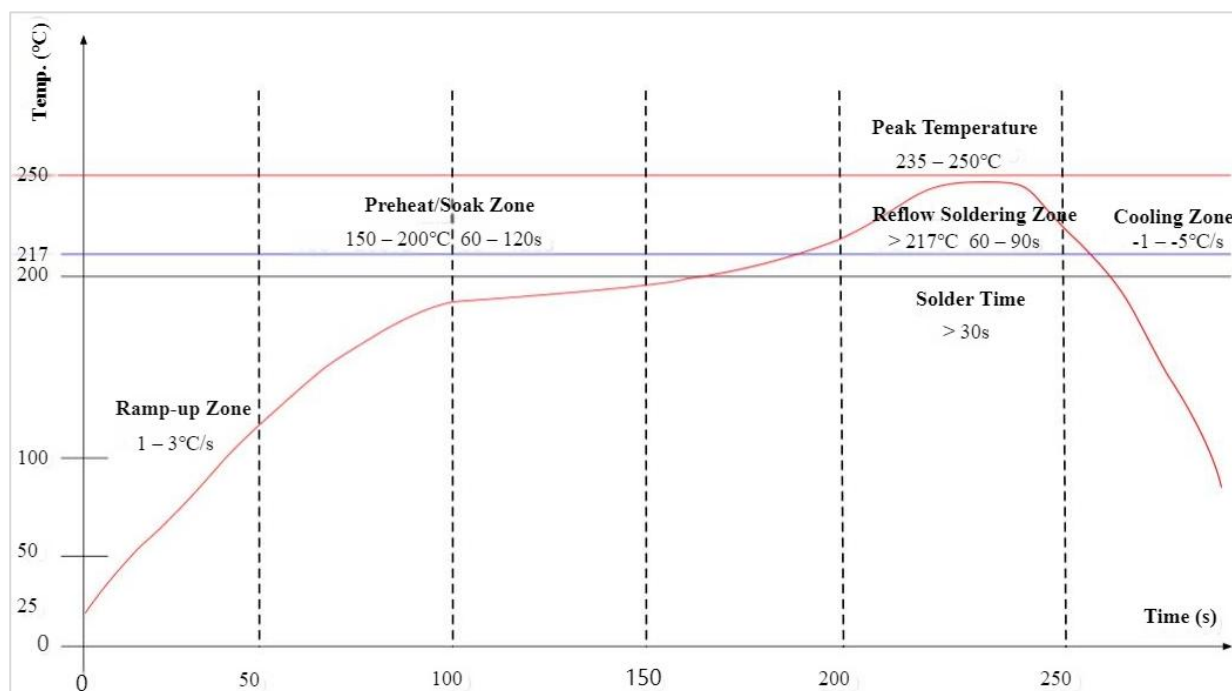


Figure 14 Reflow Soldering Profile

Reflow Soldering Profile Description:

- Ramp-up zone – Temperature: $25 - 150^{\circ}\text{C}$, Time: 60 – 90s, Ramp rate: $1 - 3^{\circ}\text{C/s}$
- Preheat/soak zone – Temperature: $150 - 200^{\circ}\text{C}$, Time: 60 – 120s
- Reflow soldering zone – Temperature: $> 217^{\circ}\text{C}$, Time: 60 – 90s, Peak temperature: $235 - 250^{\circ}\text{C}$, Time: 30 – 70s
- Cooling zone – Temperature: peak temperature to 180°C , Cooling rate: $-1 - -5^{\circ}\text{C/s}$
- Solder – Sn-Ag-Cu lead-free solder alloy (SAC305)

11 Packaging Information

Figure 15 shows the packaging of the Ai-M64L-12F module. The module is packed in tape-and-reel, 800 pcs/reel.



Figure 15 Tape and Reel Packaging Diagram

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