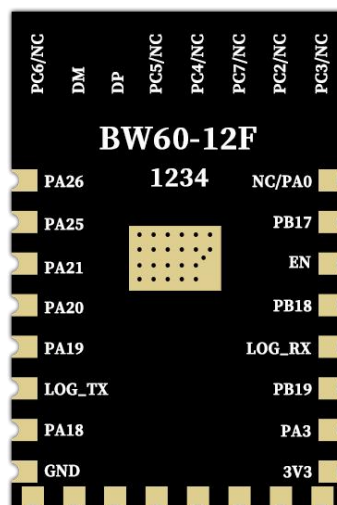
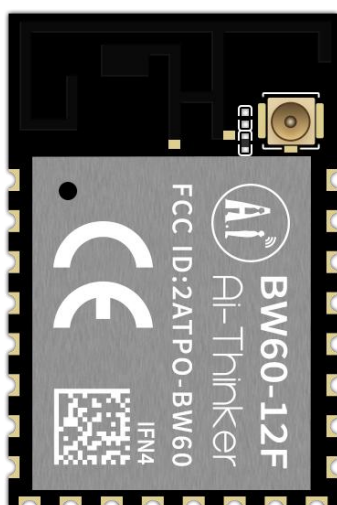


BW60-12F Specification

Version V1.0.0

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Document Revision History

Version	Date	Created / Revised Content	Prepared by	Approved by
V1.0.0	2026-04-09	First edition	Wang Yeqing	Guan Ning

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1 Product Overview

BW60-12F is a dual-band Wi-Fi + BLE SOC module developed by Ai-Thinker Technology Co., Ltd. based on the RTL8711FA chip series. It integrates Wi-Fi 6 and BLE 5.4, supporting 2.4GHz and 5GHz dual bands and 802.11 a/b/g/n/ac/ax protocols. The RTL8711FA integrates dual RISC cores compatible with Arm Cortex-M55 instruction set under Armv8.1-M architecture, with a maximum main frequency of 320MHz. It features fine-grained clock gating, multi-power modes and dynamic power adjustment, balancing high performance and ultra-low power consumption.

The BW60-12F module features a rich set of peripheral interfaces, integrating general-purpose and sensor interfaces such as UART, SPI, I2C, CAN, ADC, RMII, capacitive touch, and temperature control. It is equipped with SDIO and USB high-speed interfaces, along with DMIC and I2S audio interfaces, and the GPIOs are flexibly configurable. It can be widely applied in IoT, mobile devices, wearable electronics, smart home and other fields.

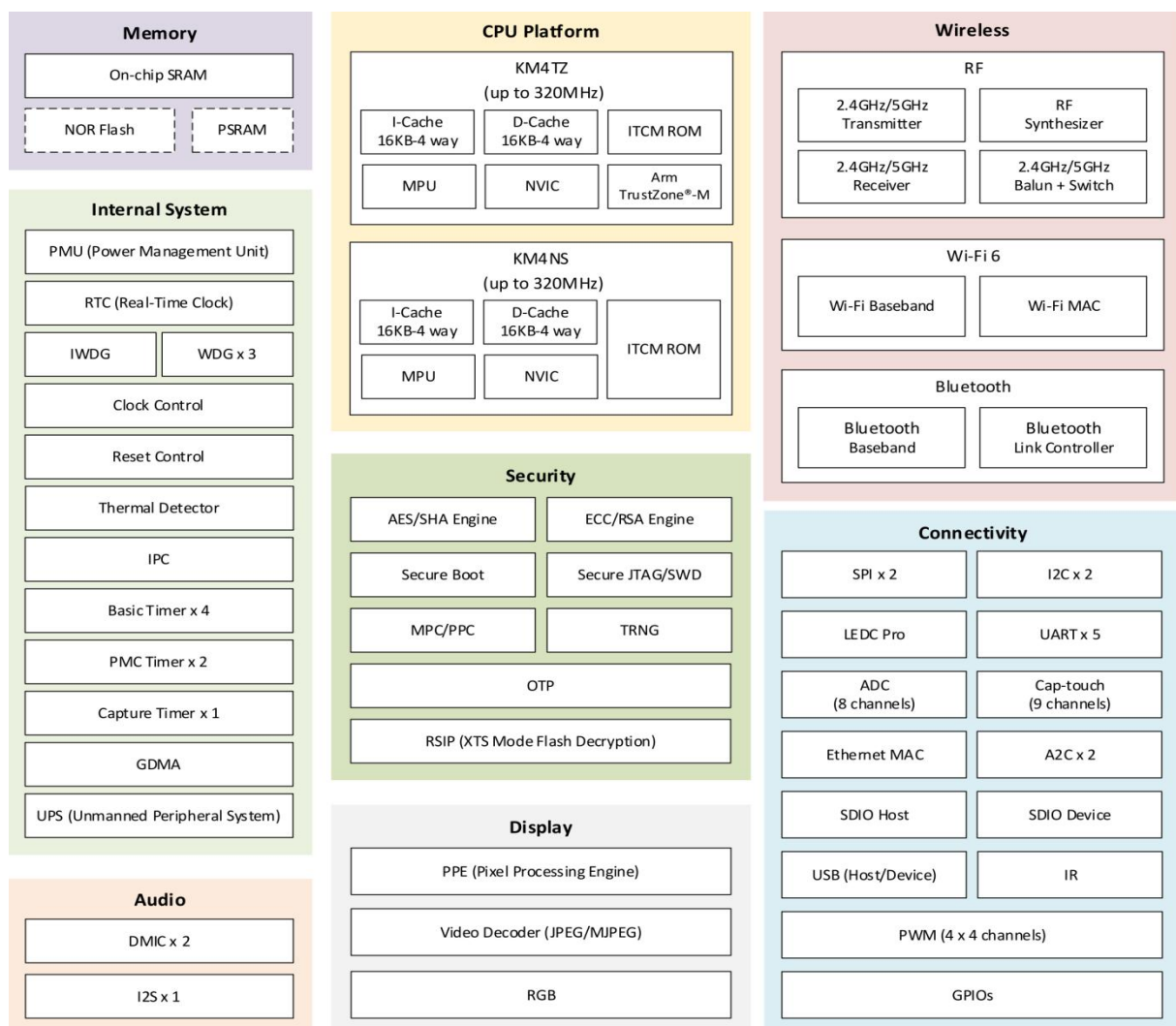


Figure 1 Main Chip Architecture Diagram

1.1 Features

Wireless

- 2.4GHz and 5GHz RF transceiver
- Supports 802.11 a/b/g/n/ac/ax protocols
- Supports BLE 5.4
- Supports LE 1Mbps, 2Mbps
- Supports LE long-range (125kbps, 500kbps)

Microcontroller Subsystem

- Dual 32-bit RISC cores based on the Armv8.1-M architecture
- Compatible with the Arm Cortex-M55 instruction set
- Maximum main frequency up to 320MHz

Security

- Supports secure boot and secure debug

- Supports Arm TrustZone®-M
- Supports AES/SHA Engine
- Supports ECC/RSA Engine
- Supports TRNG (True Random Number Generator)
- 2K bytes OTP

Peripherals

- Supports USB, SPI, UART, ADC, I2C, I2S, PWM, SDIO, LEDC, IR, RMII, and GPIO, etc.

Package Type

- Adopts SMD-24 package

Development Environment

- Supports secondary development with integrated Linux development environments

1.2 Application Scenarios

- Smart Home
- Educational/Children's Toys
- Industrial Equipment Interaction
- Wearable Electronics
- Internet of Things (IoT)
- Audio Multimedia
- Mobile Devices

2 Key Specifications

Table 1 Key Specifications

Model	BW60-12F
Package	SMD-24
Dimensions	24.0*16.0*3.2(mm)
Antenna Type	PCB onboard antenna or IPEX connector (Gen 1)
Frequency Range	2400 – 2483.5MHz and 5180 – 5825MHz
Operating Temperature	-40 – 85°C
Storage Conditions	-40 – 125°C, <90% RH
Power Supply Range	Supply voltage 2.97 – 3.63V, typical 3.3V, supply current >500mA
Supported Interfaces	USB, SPI, UART, ADC, I2C, I2S, PWM, SDIO, LEDC, IR, RMII, and GPIO, etc.
Available I/Os	21 by default
UART Baud Rate	115200bps by default
Flash	4MByte by default, up to 16MByte

3 Electrical Characteristics

3.1 Recommended Operating Conditions

Table 2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage	2.97	3.3	3.63	V
I	Supply Current	500	-	-	mA

3.2 I/O DC Electrical Characteristics

Table 3 I/O DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VIH	High-level Input Voltage	2	-	-	V
VIL	Low-level Input Voltage	-0.3	-	0.8	V
VOH	High-level Output Voltage	-	0.85*VDD	-	V
VOL	Low-level Output Voltage	-	0.15*VDD	-	V
IIN	I/O Input Leakage Current	-	-	100	nA

3.3 Electrostatic Discharge

The BW60-12F is an ESD-sensitive device and requires special precautions during handling.



Figure 2 ESD Protection Symbol

3.4 Wi-Fi RF Performance

Table 4 Wi-Fi RF Performance

Description	Typ			Unit
Frequency Range	2400 – 2483.5			MHz
2.4G Output Power				
Mode	Min	Typ	Max	Unit
802.11b, 1Mbps	-	21	-	dBm
802.11b, 11Mbps	-	20	-	dBm
802.11g, 6Mbps	-	20	-	dBm
802.11g, 54Mbps	-	18	-	dBm
802.11n, HT20 (MCS7)	-	18	-	dBm
802.11ax, HE20 (MCS9)	-	16	-	dBm
2.4G Receiver Sensitivity				
Mode	Min	Typ	Max	Unit
802.11b, 1Mbps	-	-99	-	dBm
802.11b, 11Mbps	-	-90	-	dBm
802.11g, 6Mbps	-	-95	-	dBm
802.11g, 54Mbps	-	-77	-	dBm
802.11n, HT20 (MCS7)	-	-76	-	dBm
802.11ax, HE20 (MCS9)	-	-70	-	dBm
Description	Typ			Unit
Frequency Range	5180 – 5825			MHz
5.8G Output Power				
Mode	Min	Typ	Max	Unit
802.11a, 6Mbps	-	18	-	dBm
802.11a, 54Mbps	-	18	-	dBm

802.11n, HT20 (MCS7)	-	18	-	dBm
802.11ax, HE20 (MCS9)	-	16	-	dBm
5.8G Receiver Sensitivity				
Mode	Min	Typ	Max	Unit
802.11a, 6Mbps	-	-92	-	dBm
802.11a, 54Mbps	-	-74	-	dBm
802.11n, HT20 (MCS7)	-	-72	-	dBm
802.11ax, HE20 (MCS9)	-	-63	-	dBm

3.5 BLE RF Performance

Table 5 BLE RF Performance

Description	Typ			Unit
Frequency Range	2400 – 2483.5			MHz
Output Power				
Data Rate Mode	Min	Typ	Max	Unit
1Mbps	-	8	15	dBm
2Mbps	-	8	15	dBm
Receiver Sensitivity				
Data Rate Mode	Min	Typ	Max	Unit
1Mbps Sensitivity @ 30.8% PER	-	-97	-	dBm
2Mbps Sensitivity @ 30.8% PER	-	-94	-	dBm

3.6 Power Consumption

The following power consumption data are measured under a 3.3V power supply and 25°C ambient temperature.

- The POUT power for all transmit modes is measured at the antenna interface.
- All transmission data are measured at 100% duty cycle in continuous transmit mode.

Table 6 Power Consumption

Mode	Min	Avg	Max	Unit
TX 802.11b, 11Mbps, POUT=+18dBm	-	273	-	mA
TX 802.11g, 54Mbps, POUT=+15dBm	-	267	-	mA
TX 802.11n, MCS7, POUT=+15dBm	-	212	-	mA
TX 802.11ax, MCS9, POUT=+13dBm	-	187	-	mA
RX 802.11b, Packet Length 1500 bytes	-	47	-	mA
RX 802.11g, Packet Length 1500 bytes	-	51	-	mA
RX 802.11n, Packet Length 1500 bytes	-	51	-	mA
RX 802.11ax, Packet Length 1500 bytes	-	51	-	mA
Deep-sleep		10		uA

4 Mechanical Specifications

4.1 Module Dimensions

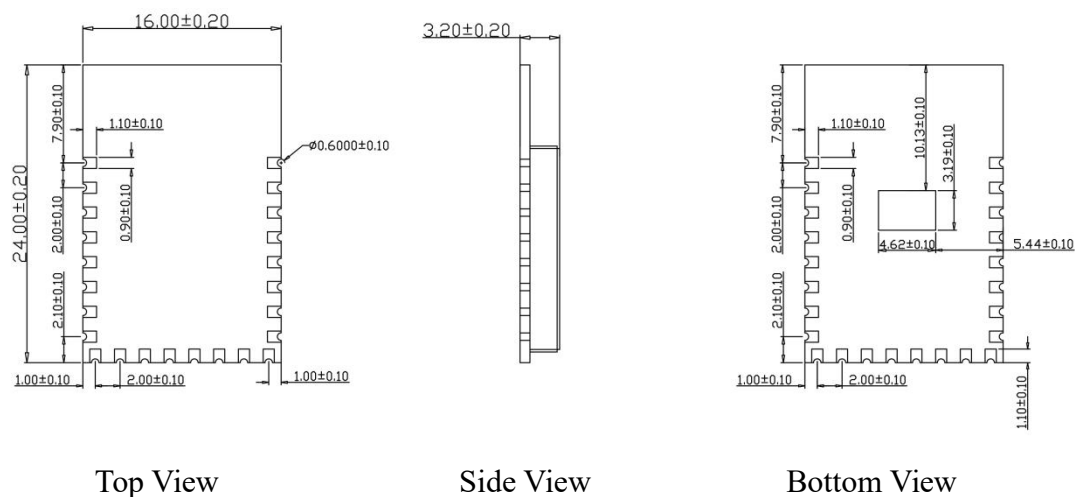


Figure 3 Module Dimensions (Unit: mm)

4.2 Shield Can Marking Information

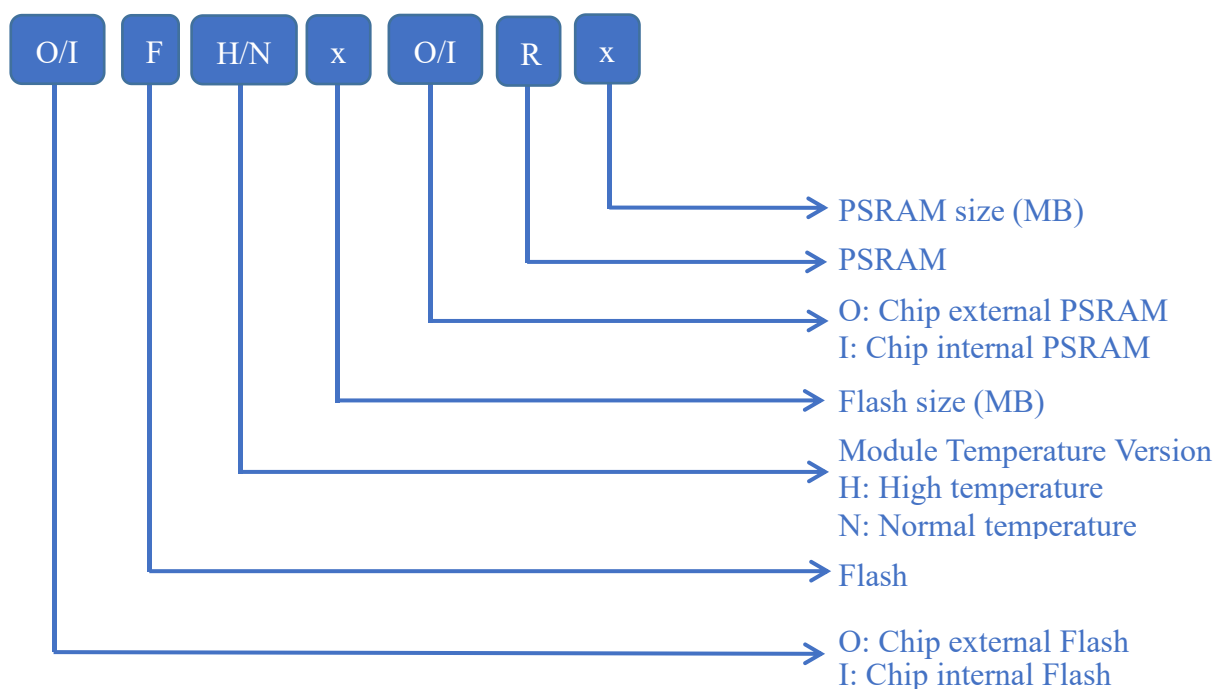


Figure 4 Shield Can Marking Information

4.3 External Antenna Connector Dimensions

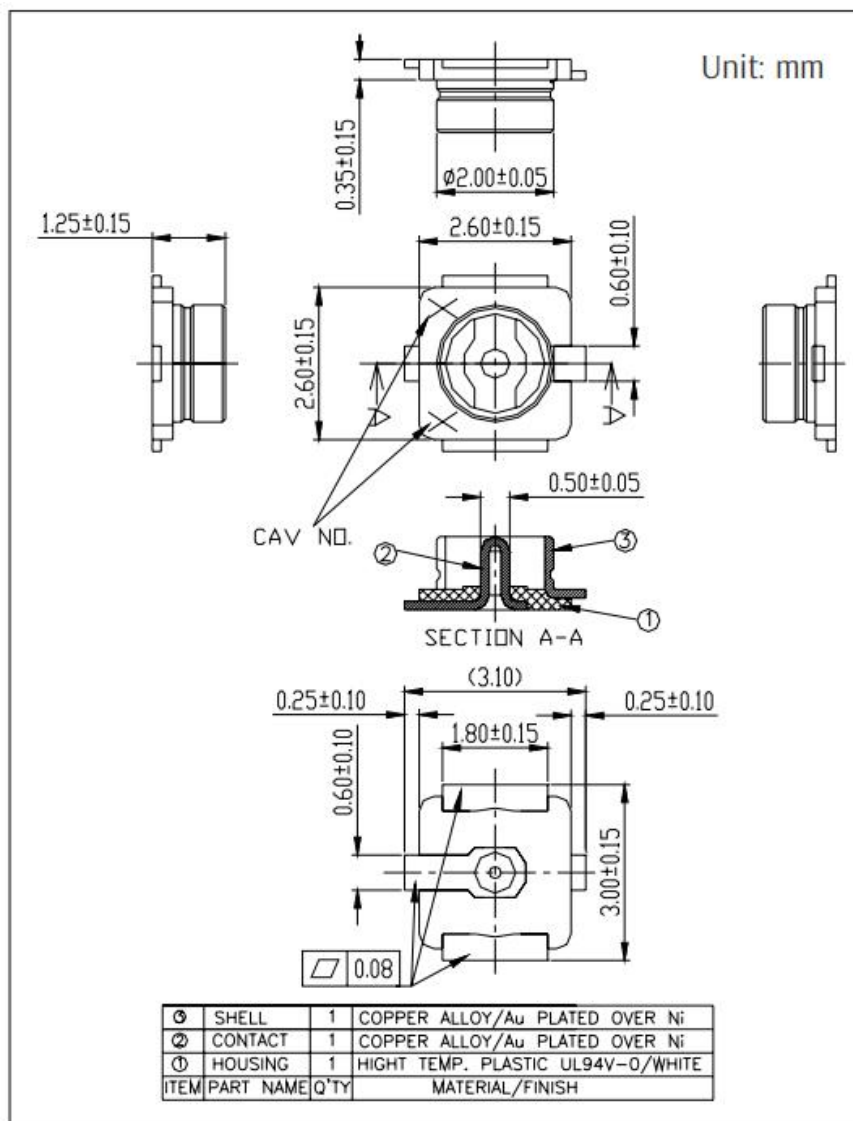


Figure 5 External Antenna Connector Dimensions (Unit: mm)

5 Pin Definition

The BW60-12F module exposes a total of 24 pins, as shown in the pin diagram. The pin function definition table provides the detailed interface specifications.

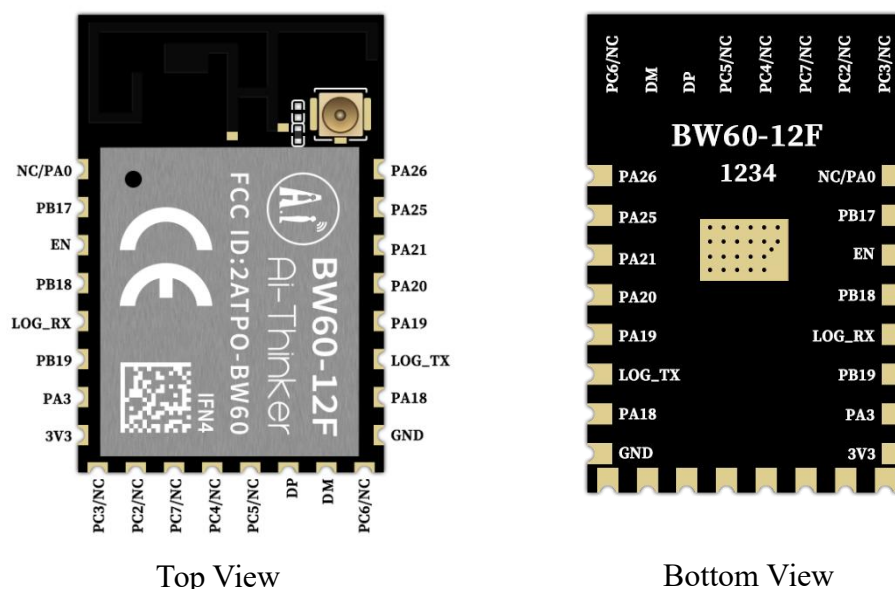


Figure 6 Pin Diagram

Table 7 Pin Function Definitions

No.	Name	Function
1	PA0/NC	GPIO/WAKE_PIN3; not available on the internal PSRAM version due to internal multiplexing
2	PB17	GPIO/RMII_RXERR
3	EN	Chip enable pin, active high
4	PB18	GPIO/RMII_REF_CLK/SWD_CLK
5	LOG_RX	PA2/OTP_DIS/WAKE_PIN1 Flashing port, LOG_RX pin
6	PB19	GPIO/RMII_RXD1/SWD_DAT
7	PA3	GPIO/WAKE_PIN0
8	3V3	3.3V supply (VDD); external power supply output current recommended above 500mA
9	PC3/NC	GPIO/RMII_TXD1/SPI1_MOSI/SD_D0; on the external Flash version, this IO is shared with internal Flash and not

		exposed
10	PC2/NC	GPIO/RMII_TXEN/SPI1_CLK/SD_D2; on the external Flash version, this IO is shared with internal Flash and not exposed
11	PC7/NC	GPIO/RMII_RXD0/SD_CLK; on the external Flash version, this IO is shared with internal Flash and not exposed
12	PC4/NC	GPIO/RMII_TXD0/SPI1_MISO/SD_D1; on the external Flash version, this IO is shared with internal Flash and not exposed
13	PC5/NC	SPIC(0/1)_FLASH_CLK/GPIO/RMII_CRS_DV/SPI1_CS/SD_D3; on the external Flash version, this IO is shared with internal Flash and not exposed
14	DP/PA4	GPIO/HSDP/SPI0_CLK/SWD_CLK/SD_D2
15	DM/PA5	GPIO/HSDM/SPI0_MOSI/SWD_DAT/SD_D0
16	PC6/NC	SPIC(0/1)_FLASH_D0/RMII_RXD1/SD_CMD; on the external Flash version, this IO is shared with internal Flash and not exposed
17	GND	Ground
18	PA18	GPIO/ADC2_TOUCH2/TSSI_0/SPI0_MISO/SWD_CLK/SD_CLK
19	LOG_TX	PB20/UD_DIS Flashing port, LOG_TX pin. Also used as a boot configuration pin; see the notes below.
20	PA19	GPIO/ADC1_TOUCH1/TSSI_1/SPI0_CS/SWD_DAT/SD_CMD
21	PA20	GPIO/ADC0_TOUCH0/SD_D1
22	PA21	GPIO/TOUCH8/SD_D3
23	PA25	GPIO/TSSI_0/RMII_RXERR
24	PA26	GPIO/TSSI_1/RMII_REF_CLK/SD_D3

Notes:

- Whether pins marked NC (no connection) are available depends on the internal PSRAM and Flash configuration of the module. On the internal PSRAM version, PA0 is unavailable. On the external Flash version, PC2, PC3, PC4, PC5, PC6, and PC7 are unavailable.
- If LOG_TX is low at the moment of power-on, the module enters flashing mode. If LOG_TX is high at the moment of power-on, the module boots normally. The module has an internal pull-up by default.
- Do not pull PA3 low at the moment of power-on. Pulling it low during startup will cause the module to enter Test Mode.
- Do not pull PB18 low at the moment of power-on. Pulling it low will prevent the NOR Flash from booting. The module has an internal pull-up by default.

6 Schematic

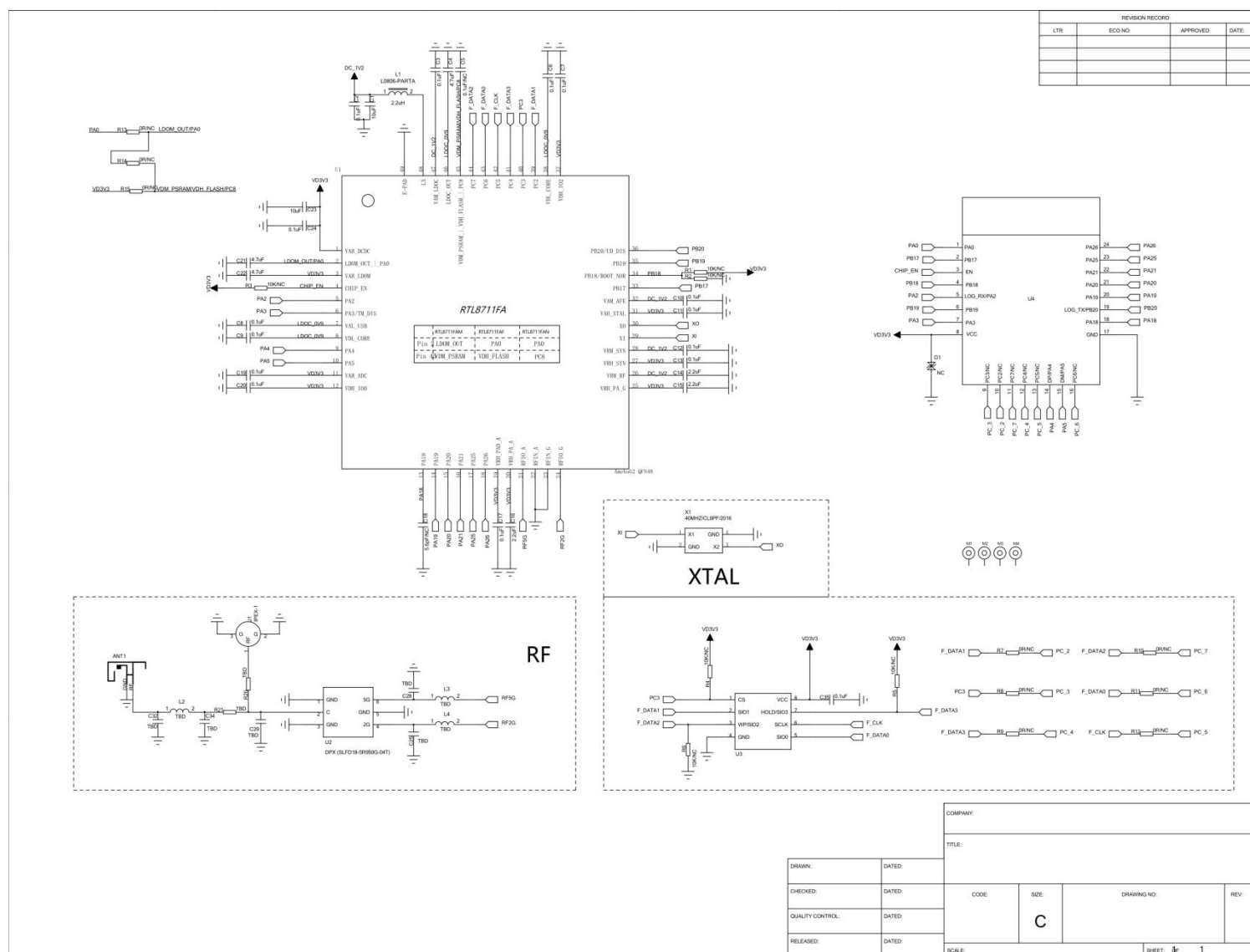


Figure 7 Schematic

7 Antenna Parameters

7.1 Antenna Test Prototype

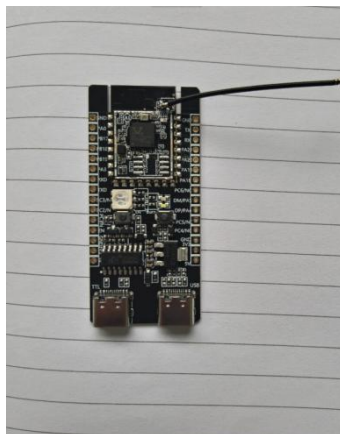


Figure 8 Antenna Test Prototype

7.2 Antenna S-Parameters

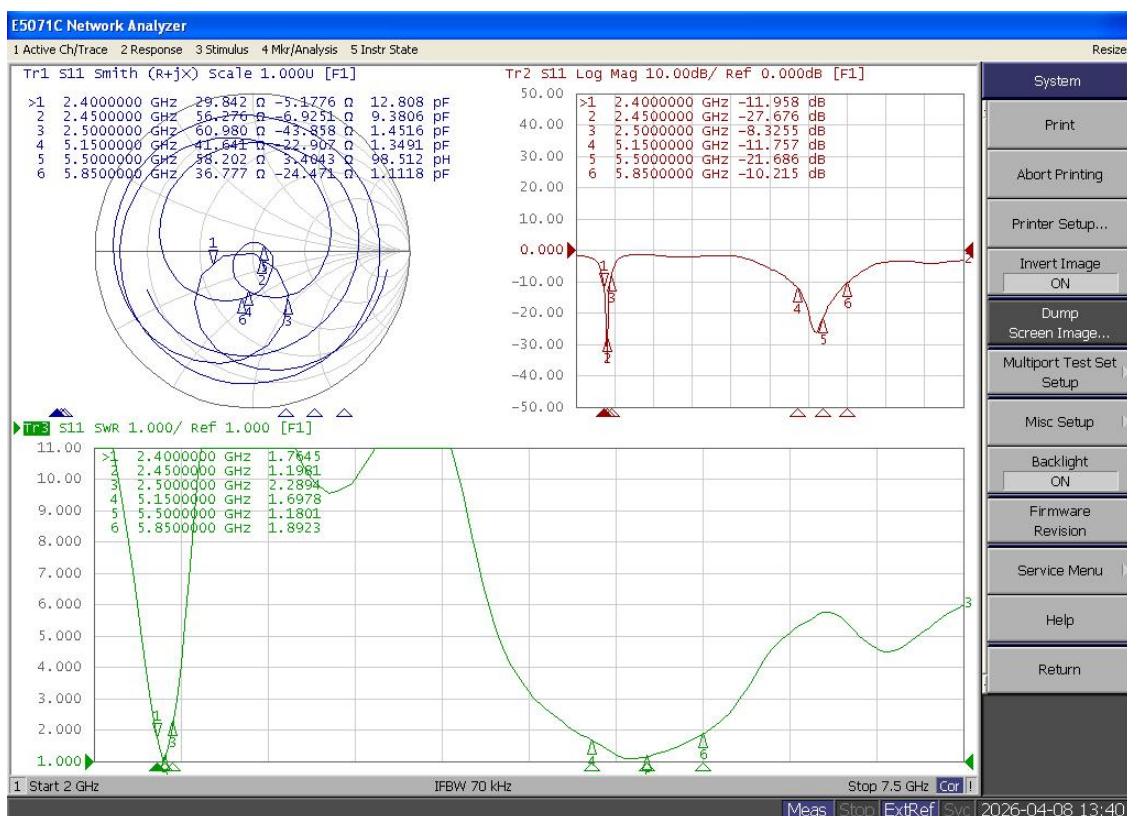


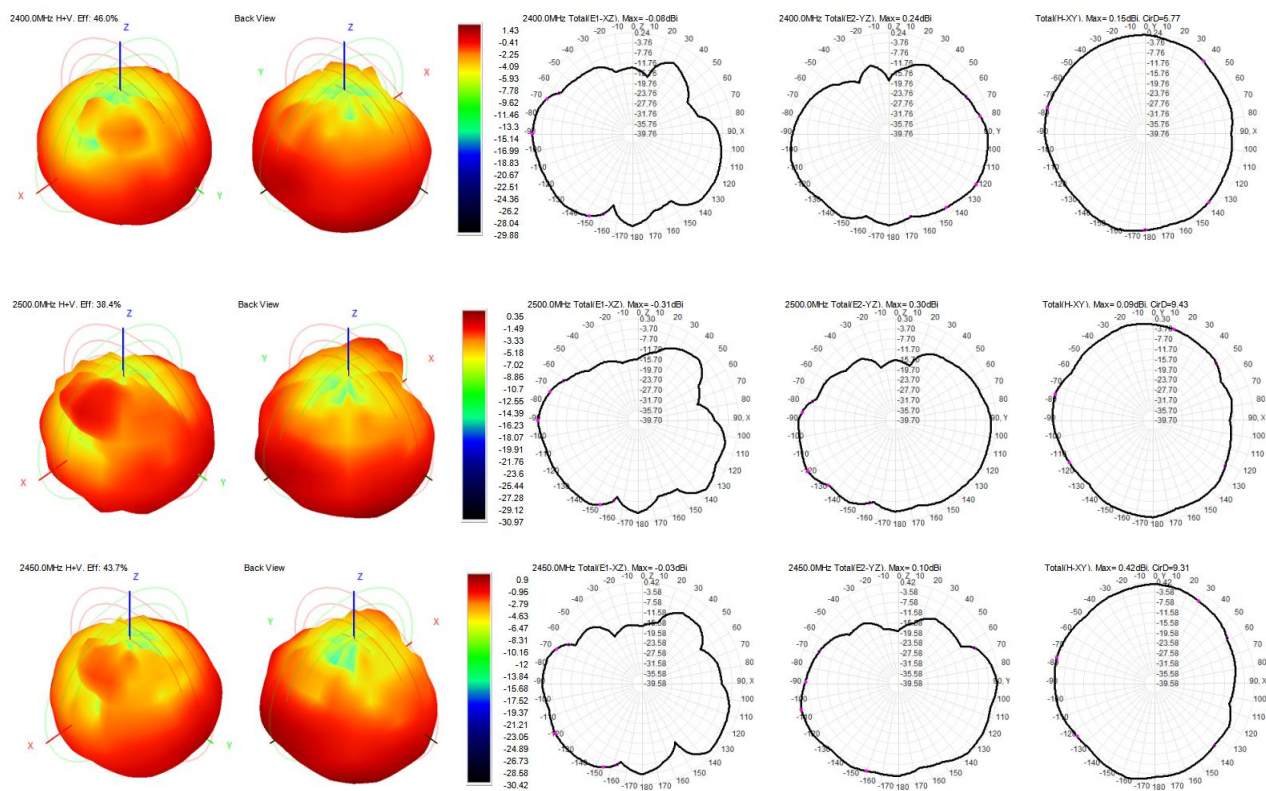
Figure 9 Antenna S-Parameters

7.3 Antenna Gain and Efficiency

Table 8 Antenna Gain and Efficiency

No.	1	2	3	4	5	6	7	8	9	10	11
Frequency (MHz)	2400	2410	2420	2430	2440	2450	2460	2470	2480	2490	2500
Gain (dBi)	1.43	1.45	1.35	1.71	1.45	0.90	1.04	1.86	1.13	1.07	0.35
Efficiency (%)	46.03	46.91	45.16	45.80	44.79	43.74	43.75	44.09	42.29	41.12	38.45
Frequency (MHz)	5150	5250	5350	5450	5550	5650	5750	5850	-	-	-
Gain (dBi)	2.45	3.18	3.53	4.06	3.04	5.28	4.60	4.54	-	-	-
Efficiency (%)	52.37	58.29	61.85	72.25	61.02	62.50	63.49	60.62	-	-	-

7.4 Antenna Pattern Diagram



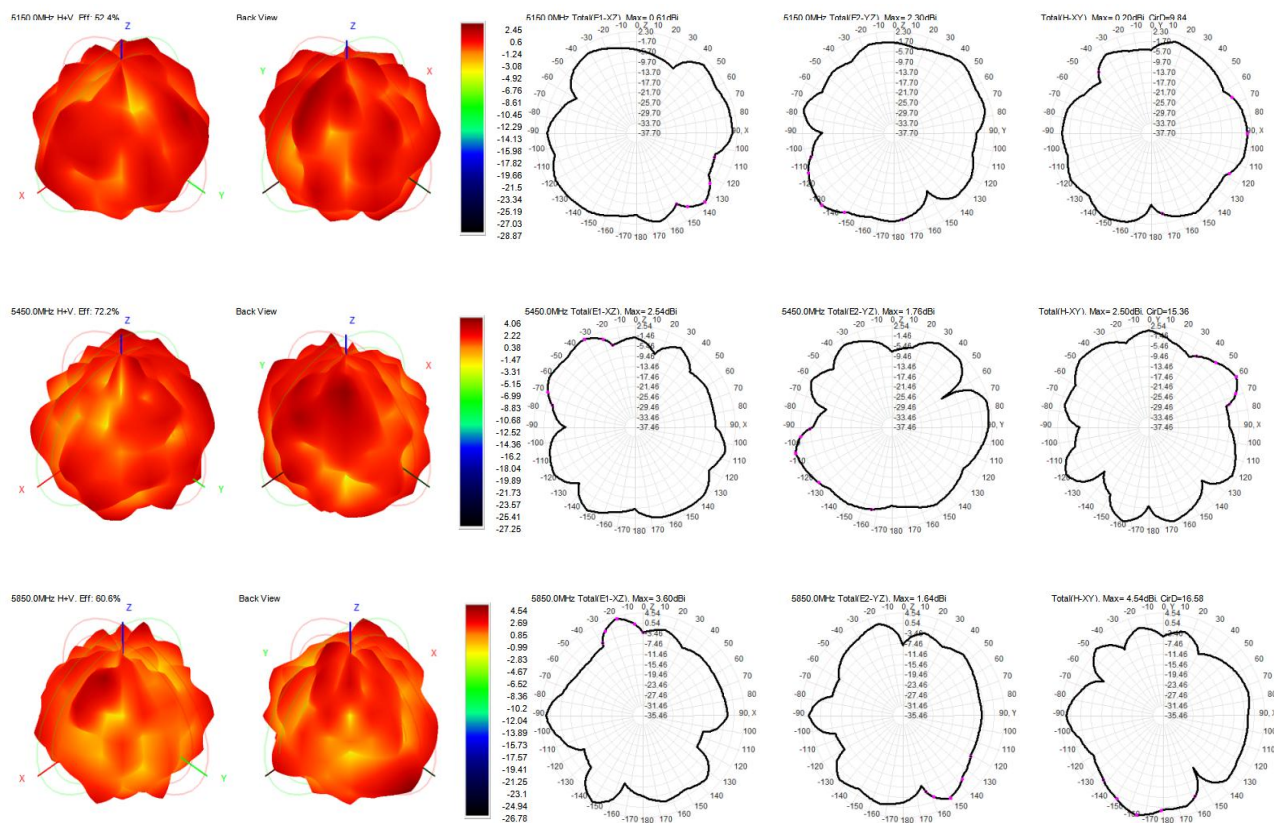


Figure 10 Antenna Pattern Diagram

8 Design Guide

8.1 Application Reference Circuit

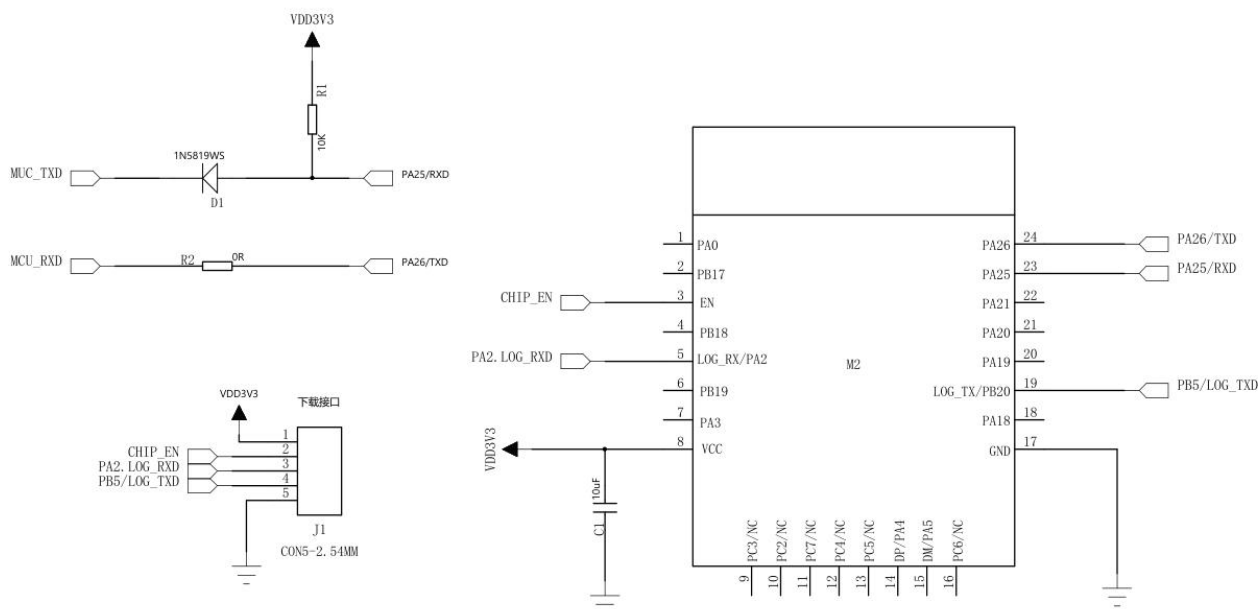


Figure 11 Application Reference Circuit

- LOG_TX is the boot control pin. When high, the module is in normal operating mode. When low, the module is in firmware flashing mode. The chip is internally pulled high by default.
- VDD3V3 supply voltage: 2.97 – 3.63V. The external power supply output current is recommended to be above 500mA.

8.2 Recommended PCB Footprint Dimensions

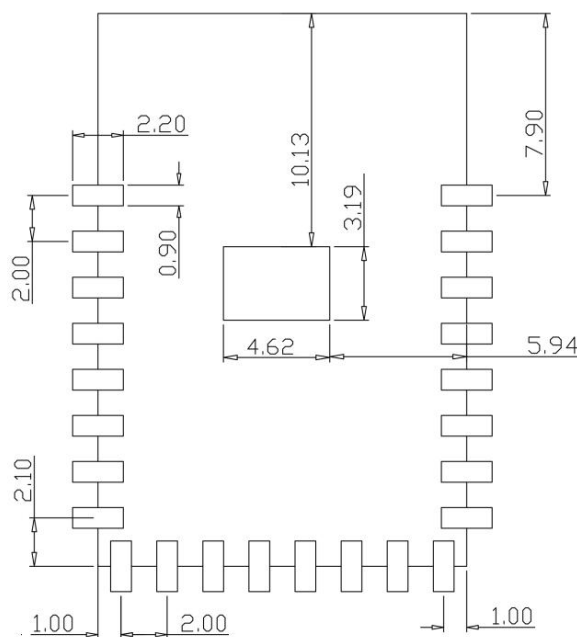


Figure 12 Recommended PCB Footprint Dimensions (Unit: mm)

8.3 Antenna Layout Requirements

- For the installation position on the mainboard, the following 2 options are recommended.

Option 1: Place the module at the mainboard edge, with the antenna area extending beyond it.

Option 2: Place the module at the mainboard edge, with a clearance cutout at the antenna position.

- To ensure optimal performance of the onboard antenna, metal objects must not be placed near the antenna, and the antenna should be kept away from high-frequency devices.

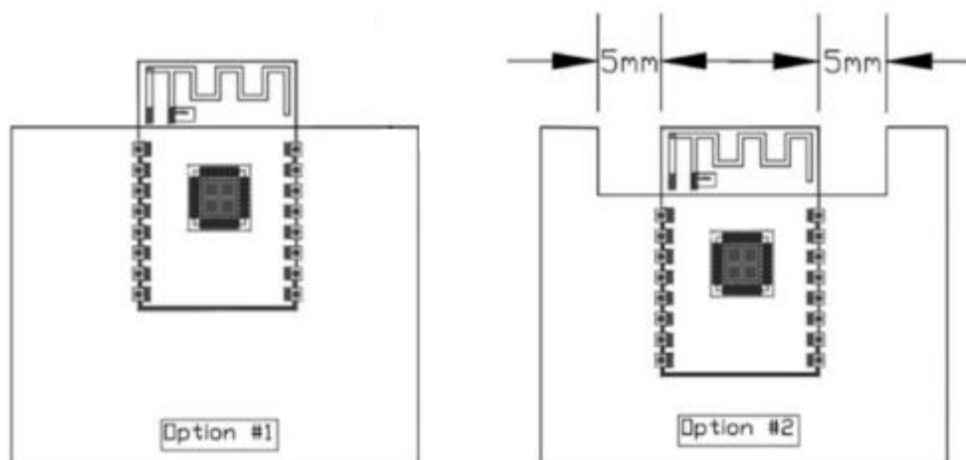


Figure 13 Antenna Layout Diagram

8.4 Power Supply

- VDD is recommended as 3.3V, with a peak current above 500mA.
- An LDO is recommended for power supply; if using DC-DC, the ripple should be controlled within 30mV.
- For the DC-DC power supply circuit, it is recommended to reserve space for dynamic response capacitors to optimize output ripple under large load transients.
- It is recommended to add ESD protection devices to the power interface.

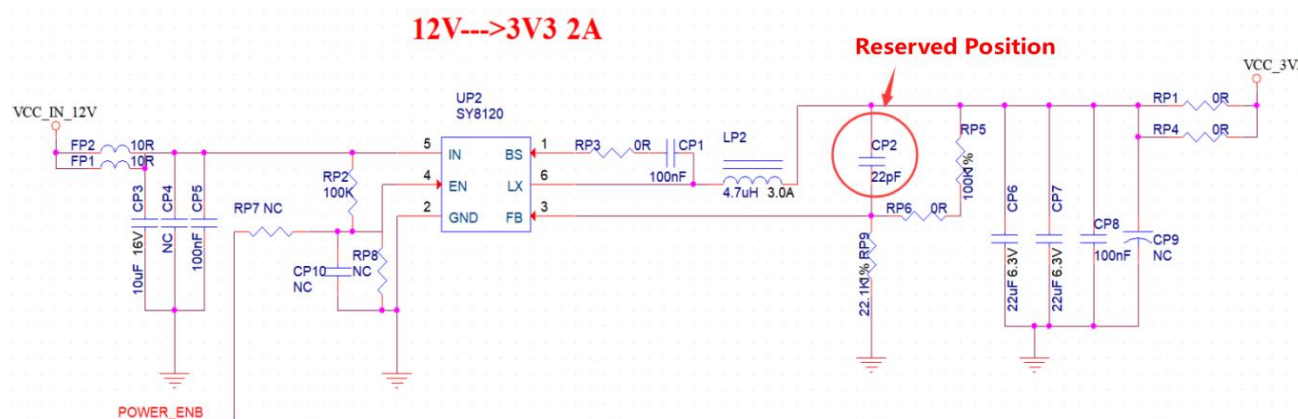


Figure 14 DC-DC Buck Circuit

8.5 GPIO

- Some I/O pins are exposed on the module periphery. To use these I/O pins, it is recommended to connect a 10-100Ω resistor in series with each I/O pin. This helps suppress overshoot, stabilize signal levels, and benefits both EMI and ESD protection.
- The pull-up or pull-down configuration for special I/O pins must refer to the instructions in the specification, as it affects the module boot configuration.
- The module I/O pins level is 3.3V. If the host controller I/O voltage level does not match the module, a level-shifting circuit should be added.
- If an I/O pin is directly connected to a peripheral interface or pin headers, it is recommended to reserve space for an ESD protection device near the connector on the I/O trace.

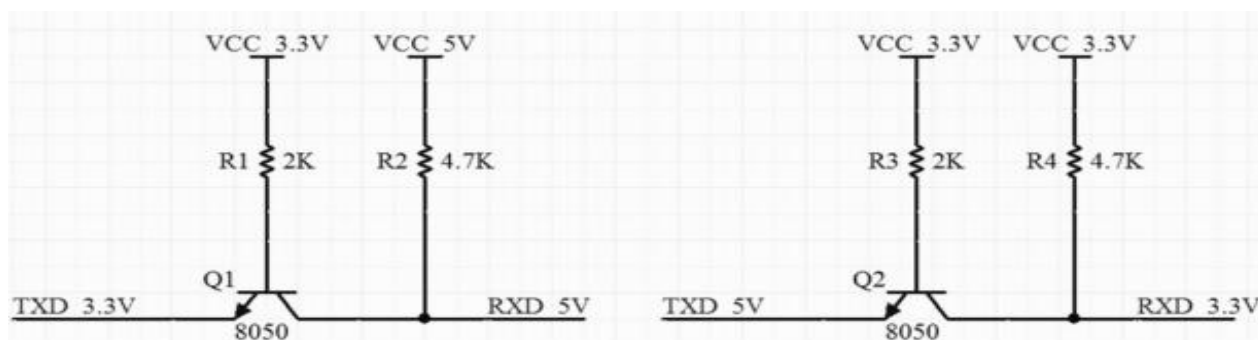


Figure 15 Level-shifting Circuit

9 Storage Conditions

Products sealed in moisture barrier bags should be stored in a non-condensing atmosphere at $< 40^{\circ}\text{C}$ and $< 90\% \text{ RH}$.

The moisture sensitivity level (MSL) of the module is level 3.

The module must be used within 168 hours after vacuum bag removal under conditions of $25 \pm 5^{\circ}\text{C}$ and 60% RH. Otherwise, the module requires baking before being returned to production.

10 Reflow Soldering Profile

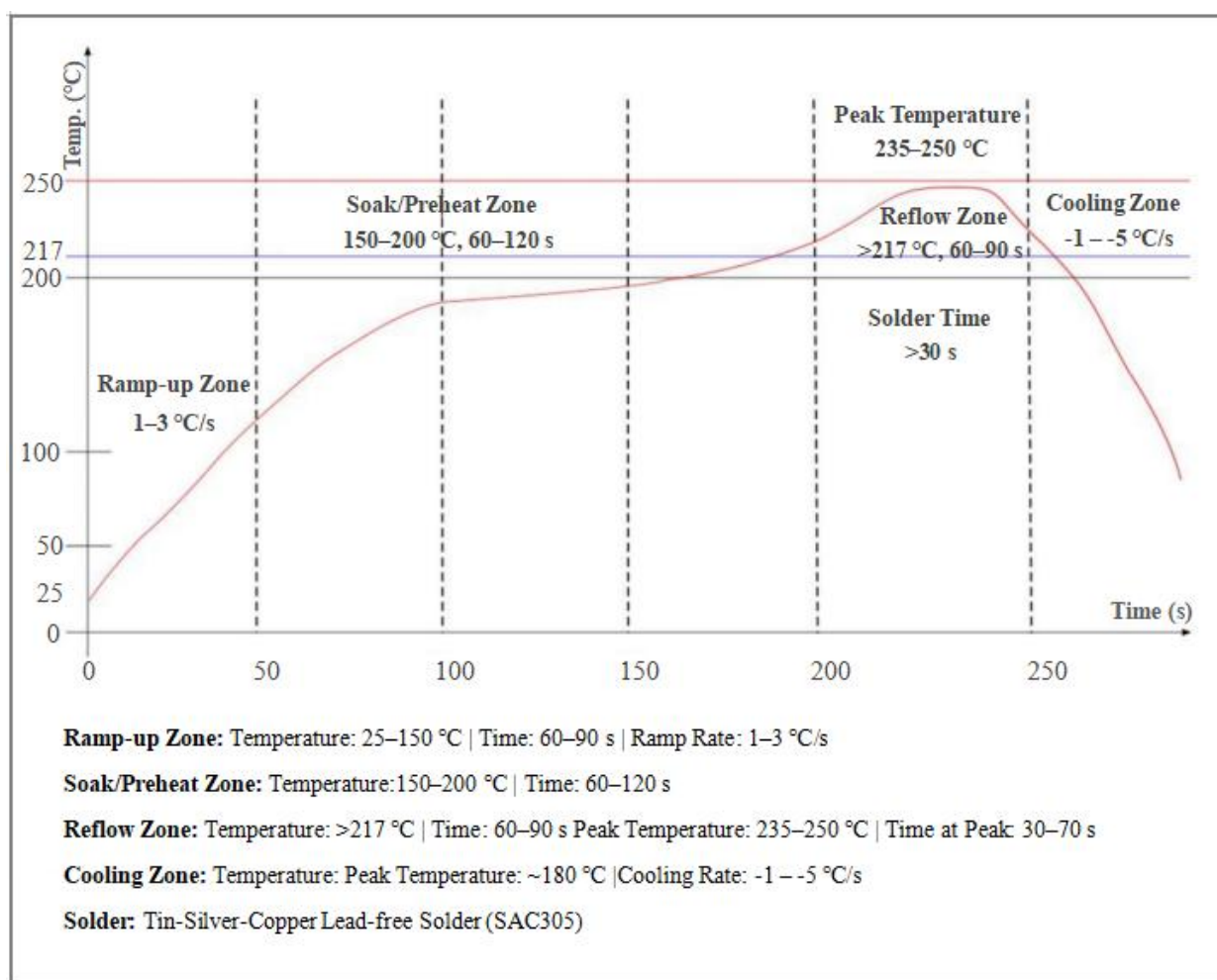


Figure 16 Reflow Soldering Profile

11 Packaging Information

The BW60-12F module is packaged in tape and reel, 800 pcs/reel.



Figure 17 Tape and Reel Packaging Diagram

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