Ai-WB3-12F Specification

Version V1.0.0

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Document resume

Version	Date	Develop/revise content	Edition	Approve
V1.0.0	2023.2.3	First Edition	JiYe Yang	NingGuan

Content

1. Product Overview

Ai-WB3-12F is a Wi-Fi&BLE module developed by Shenzhen Ai-Thinker Technology Co., Ltd. The module is equipped with LN882H chip as the core processor and supports Wi-Fi 802.11b/g/n protocol and BLE 5.1 protocol. The LN882H chip integrates the Cortex-M4F core, with a maximum frequency of 160MHz, built-in 296KB SRAM, 128KB ROM and rich peripheral interfaces, including SDIO/SPI/UART/I2C/PWM/ADC/DMA/SWD/GPIO, etc. It can be widely used in Internet of Things (IoT), mobile devices, wearable electronic devices, smart home and other fields.

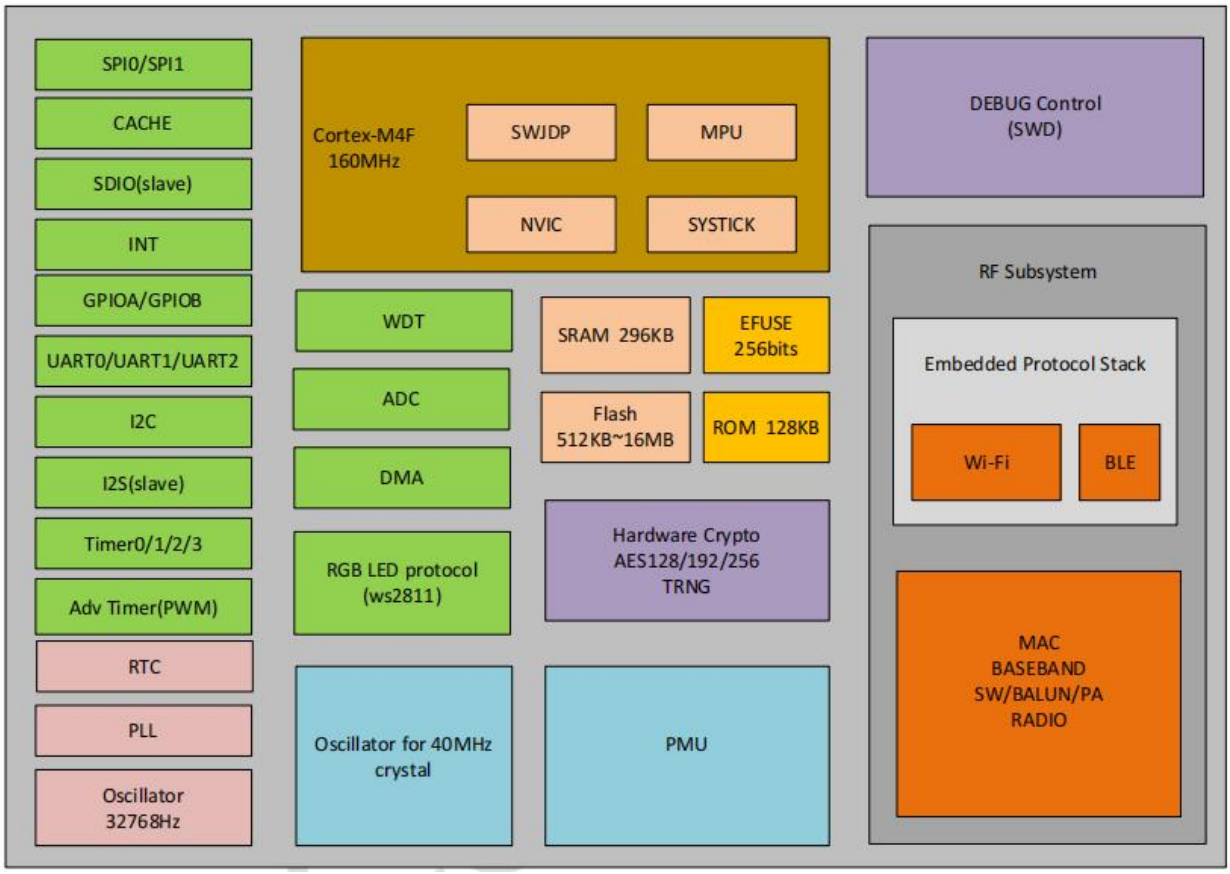


Figure 1 Main chip architecture diagram

1.1. Characteristic

- The package is SMD-22
- Support IEEE 802.11 b/g/n protocol
- Support BLE5.1
- Support long range (125Kbps, 500Kbps) and high data rate (2Mbps)
- Support 296KB SRAM / 128KB ROM
- Support SDIO/SPI/UART/I2C/PWM/ADC/DMA/SWD/GPIO port
- Supports multi-channel ADC and programmable amplifier for sound sensors
- Support RTC real-time clock and WDT watchdog
- Supports True Random Number Generator (TRNG)
- Support AES-128\AES-192\AES-256 hardware encryption
- Support 256 bits EFUSE
- Integrated CHKSUM accelerator to improve TCP/UDP transmission

2. Main parameters

Table 1 Description of the main parameters

Model	Ai-WB3-12F
Package	SMD-22
Size	24.0*16.0*3.1(±0.2)mm
Antenna	on-board PCB antenna
Frequency	2400 ~ 2483.5MHz
Operating temperature	-40℃ ~ 85℃
Storage temperature	-40℃ ~ 125℃, < 90%RH
Power supply	Support voltage 2.7V ~ 3.6V,supply current ≥500mA
Interface	SDIO/SPI/UART/I2C/PWM/ADC/DMA/SWD/GPIO
IO	19
UART rate	Default 115200 bps
Security	AES-128\AES-192\AES-256 Hardware Encryption
Flash	Default 2MByte

2.1. Static electricity requirement

Ai-WB3-12F is an electrostatic sensitive device. Therefore, you need to take special precautions when carrying it.

Figure 2 ESD preventive measures

2.2. Electrical characteristics

Table 2 Electrical characteristics table

Parameters		Condition	Min.	Typical value	Max.	Unit
Voltage Supply		VDD	2.7	3.3	3.6	V
I/O	VIL	-	-0.3	0	0.6	V
	VIH	-	VIO-0.6	VIO	VIO+0.3	V
	VOL	-	-0.45	0	0.45	V
	VOH	-	VIO-0.5	VIO	VIO+0.5	V

2.3. Wi-Fi RF Performance

Table 3 Wi-Fi RF performance table

Description	Typical value			Unit
Frequency range	2400 ~ 2483.5MHz			MHz
Output Power				
Mode	**Min.**	**Typical value**	**Max.**	**Unit**
11n Mode HT20，PA output power	-	14	-	dBm
11g Mode, PA output power	-	16	-	dBm
11b Mode, PA output power	-	18	-	dBm
Receive Sensitivity				
Mode	**Min.**	**Typical**	**Max.**	**Unit**
11b，1 Mbps	-	-95	-	dBm
11b，11 Mbps	-	-88	-	dBm
11g，6 Mbps	-	-91	-	dBm
11g，54 Mbps	-	-74	-	dBm
11n，HT20 (MCS7)	-	-71	-	dBm

2.4. BLE RF Performance

Table 4 BLE RF performance table

Description	Typical value			Unit
Frequency range	2400 ~ 2483.5MHz			MHz
Output Power				
Rate Mode	**Min.**	**Typical value**	**Max.**	**Unit**
1Mbps	-	12	-	dBm
Receive Sensitivity				
Rate Mode	**Min.**	**Typical value**	**Max.**	**Unit**
1Mbps sensitivity@30.8%PER	-	-95	-	dBm

2.5. Power

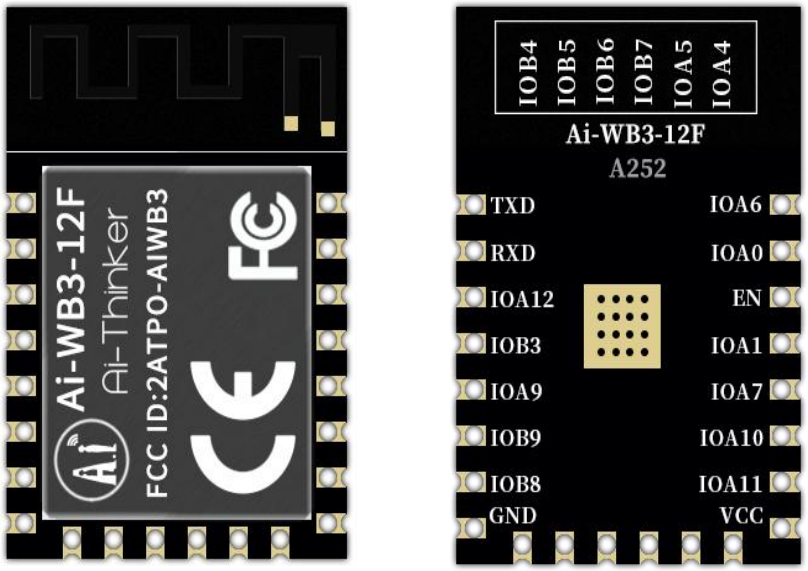
The following power consumption data is based on a 3.3V power supply and an ambient temperature of 25° C.

- All POUT power for all emission modes is measured at the antenna interface.
- All emission data is based on 95% of the duty ratio, measured in continuous emission mode.

Table 5 Power consumption

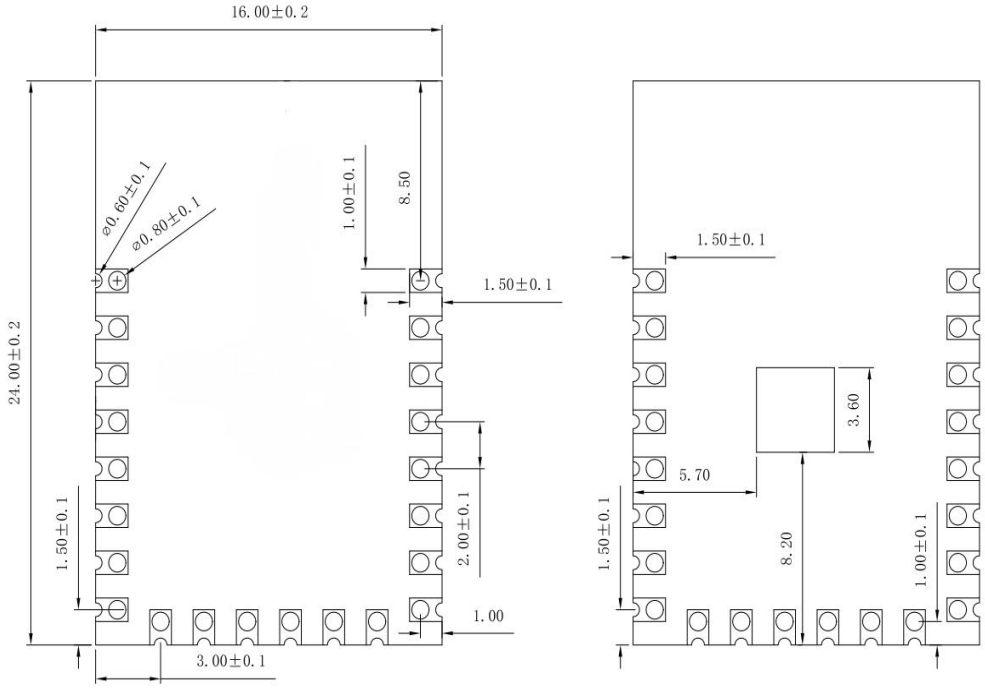
Mode		Min.	AVG	Max.	Unit
Tx 802.11b，11Mbps，POUT=+18dBm		-	260	-	mA
Tx 802.11g， 54Mbps， POUT =+16dBm		-	235	-	mA
Tx 802.11n， MCS7， POUT =+14dBm		-	225	-	mA
Rx 802.11b，packet length 1024 byte		-	90	-	mA
Rx 802.11g，packet length 1024 byte		-	90	-	mA
Rx 802.11n，packet length 1024 byte		-	90	-	mA
Sleep Mode	DTIM=1	-	11	-	mA
	DTIM=3	-	8	-	mA

3. Appearance Dimensions



Front Back

Figure 3 Appearance (the rendering is for reference only, the actual object shall prevail)

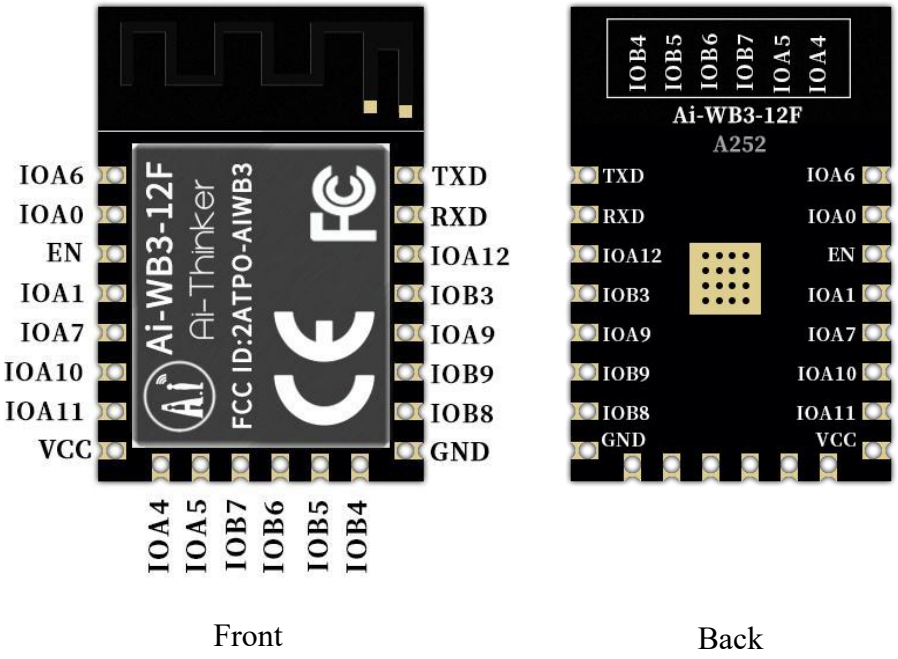


Front Back

Figure 4 Dimension diagram（unit：mm）

4. Pin Definition

The Ai-WB3-12F module has a total of 22 pins, as shown in the schematic diagram of the pins, and the pin function definition table is the interface definition.



Front Back

Figure 5 pin diagram

Table 6 Pin function definition table

No.	Name	Function Description
1	IOA6	GPIOA6/SDIO_IO2/I2S_SDI/EXT_INT/FULLMUX
2	IOA0	GPIOA0/ADC/EXT_INT/FULLMUX
3	EN	Default chip enable pin, active-high.
4	IOA1	GPIOA1/ADC/SWD/EXT_INT/FULLMUX
5	IOA7	GPIOA7/SDIO_IO3/EXT_INT/FULLMUX
6	IOA10	GPIOA10/SDIO_IO0/I2S_SDO/FULLMUX
7	IOA11	GPIOA11/SDIO_IO1/FULLMUX
8	VCC	3.3V power supply; the output current of the external power supply is recommended to be above 500mA
9	IOA4	GPIOA4/ADC/SWCK/FULLMUX
10	IOA5	GPIOA5/EXT_INT/FULLMUX
11	IOB7	GPIOB7/FULLMUX
12	IOB6	GPIOB6/FULLMUX
13	IOB5	GPIOB5/ADC/FULLMUX
14	IOB4	GPIOB4/ADC/FULLMUX
15	GND	Ground
16	IOB8	GPIOB8/FULLMUX
17	IOB9	GPIOB9/FULLMUX/EXT_INT
18	IOA9	GPIOA9/SDIO_CLK/I2S_SCLK/FLLMUX/BOOT_MODE
19	IOB3	GPIOB3/ADC/FULLMUX
20	IOA12	GPIOA12/FULLMUX
21	RXD	RXD/GPIOA3/EXT_INT/FULLMUX
22	TXD	TXD/GPIOA2/EXT_INT/FULLMUX
Note: 1. IOA9 is used as Bootstrap. When the power is low at the moment of power-on, the module enters the programming mode; when the power is high at the moment of power-on, the module starts normally. The module supports 1 master/slave I2C interface and 2 SPI interfaces, and any two pins with FULLMUX characteristics can be configured as I2C and SPI.		

5. Schematic

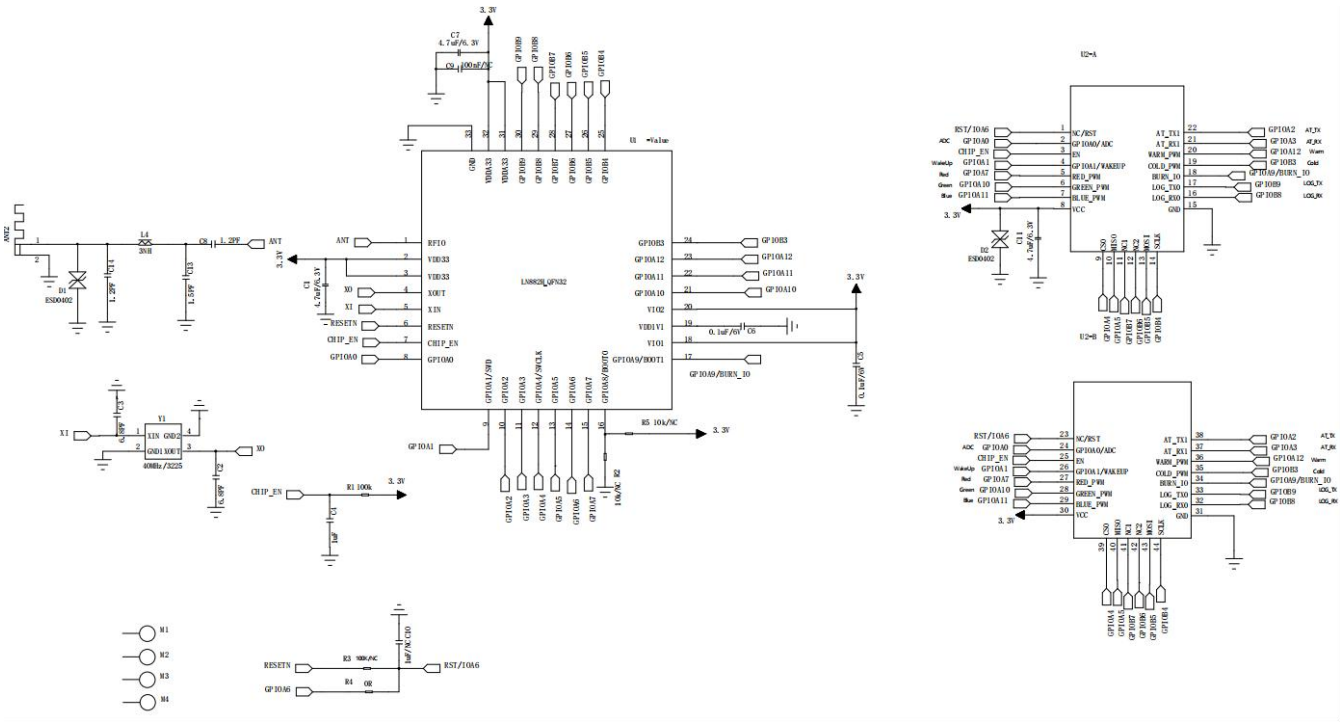


Figure 6 Module schematic

6. Antenna parameters

6.1. Schematic diagram of the antenna test prototype

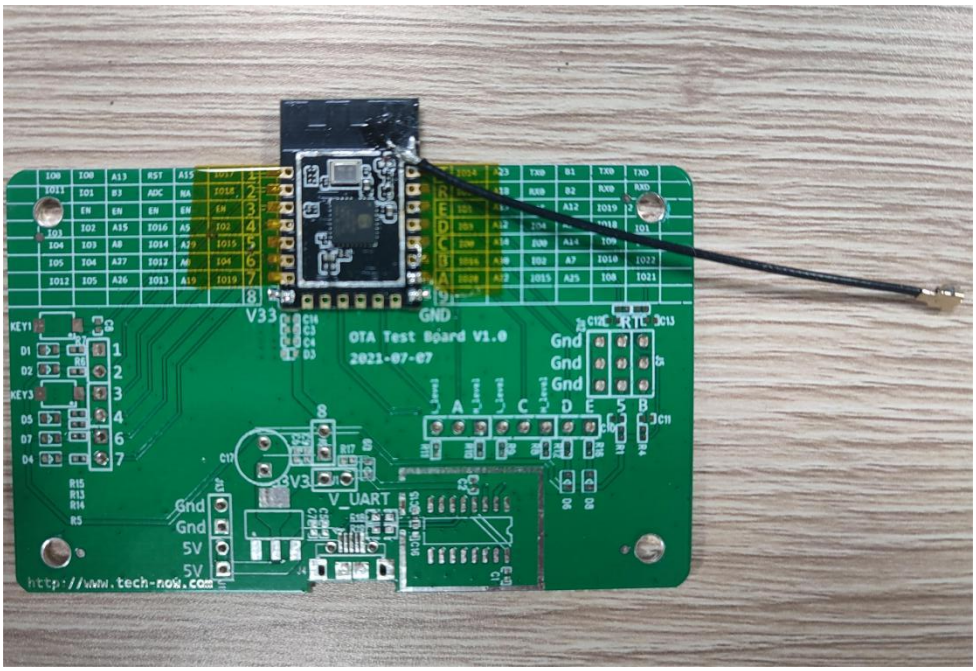


Figure 7 Schematic diagram of the antenna test prototype

6.2. Antenna S parameter

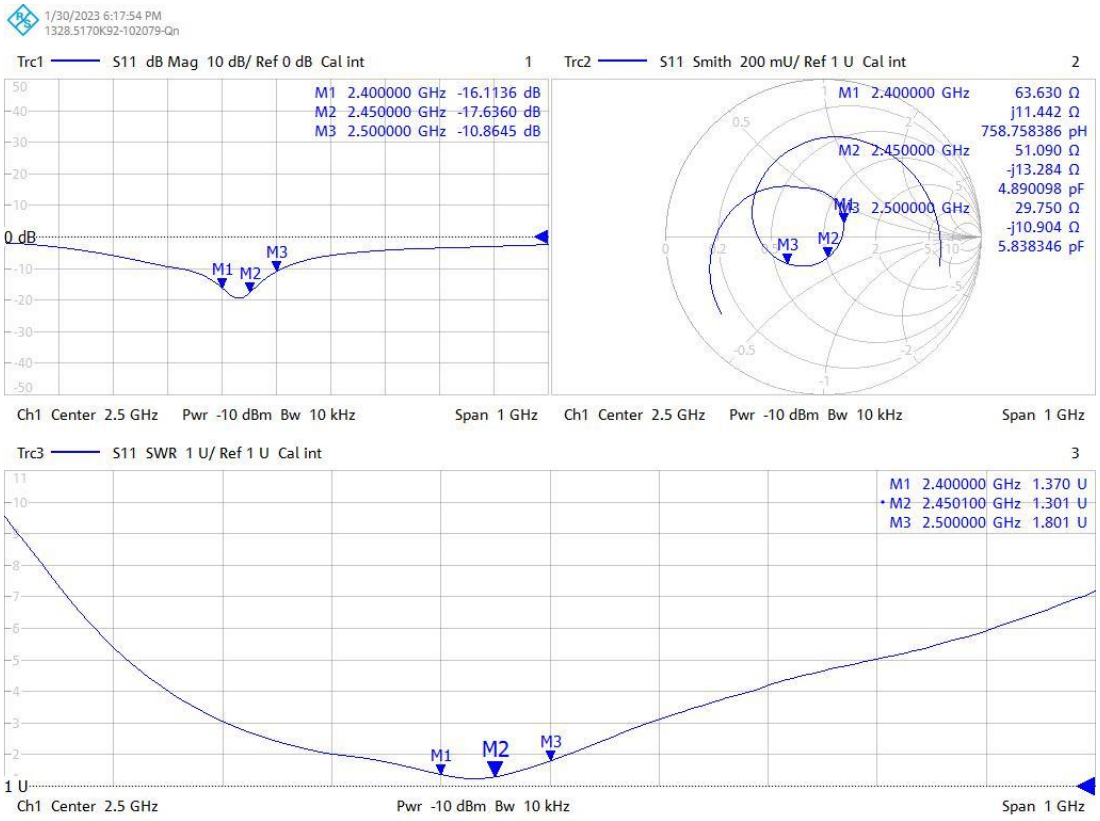


Figure 8 Antenna S parameters

6.3. Antenna Gain and Efficiency

Table 7 Antenna Gain and efficiency

Frequency ID	1	2	3	4	5	6	7	8	9	10	11
Frequency(MHz)	2400	2410	2420	2430	2440	2450	2460	2470	2480	2490	2500
Gain (dBi)	1.31	1.29	1.16	1.06	1.09	1.17	1.26	1.42	1.33	1.22	1.18
Efficiency (%)	59.9	60.6	60.1	59.8	60.8	60.8	61.8	62.3	60.2	58.8	59.7

6.4. Antenna pattern

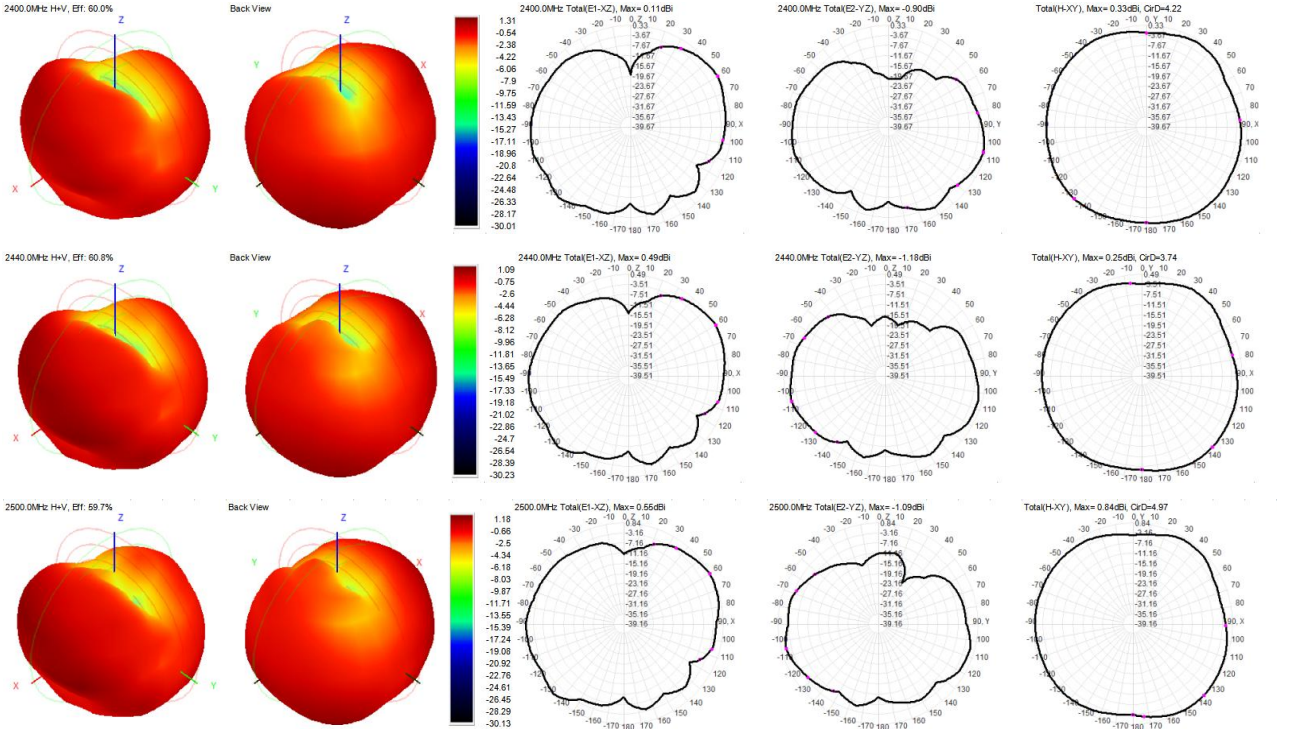


Figure 9 Antenna pattern

7. Design Guidance

7.1. Application Guide Circuit

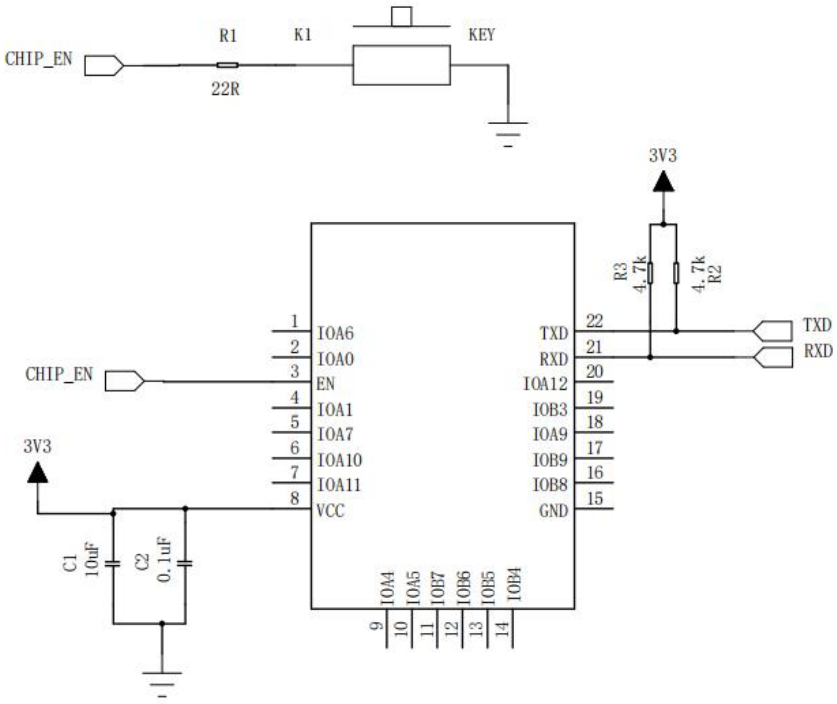


Figure 10 Application circuit diagram

- If the I/O port is used as PWM, it is recommended to reserve 4.7K pull-down resistance around the module. In particular, the application of the lamp control side prevents the flash phenomenon at the moment of power-on startup.

7.2. Recommend PCB footprint size

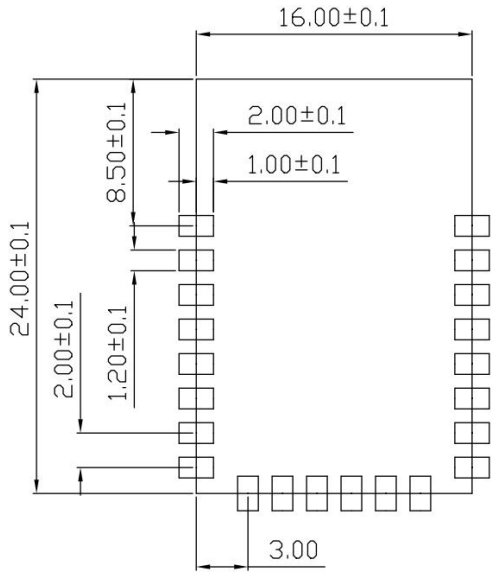


Figure 11 Recommend PCB footprint size(unit:mm)

7.3. Antenna layout requirements

- For the installation position on the motherboard, the following two methods are recommended:

Solution 1: Put the module on the edge of the motherboard, and the antenna area extends out of the edge of the motherboard.

Solution 2: Put the module on the edge of the motherboard, and hollow out an area on the edge of the motherboard where the antenna is.

- In order to meet the performance of the on-board antenna, it is forbidden to place metal parts around the antenna and keep away from high-frequency devices.

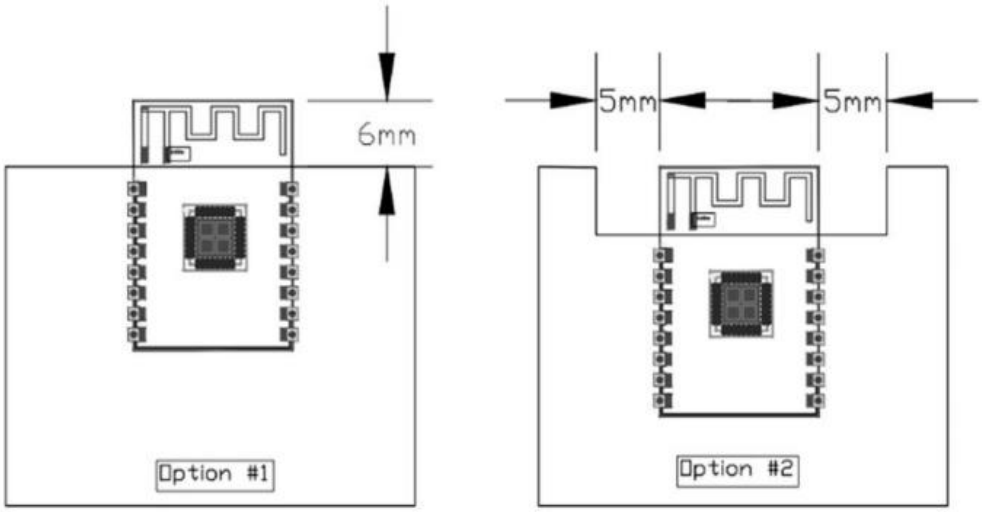


Figure 12 Antenna layout diagram

7.4. Power supply

- Recommended 3.3V voltage, peak current above 500mA.
- It is recommended to use LDO power supply; if using DC-DC, it is recommended to control the ripple within 30mV.
- It is recommended to reserve the position of the dynamic response capacitor for the DC-DC power supply circuit, which can optimize the output ripple when the load changes greatly.
- It is recommended to add ESD devices to the 3.3V power interface

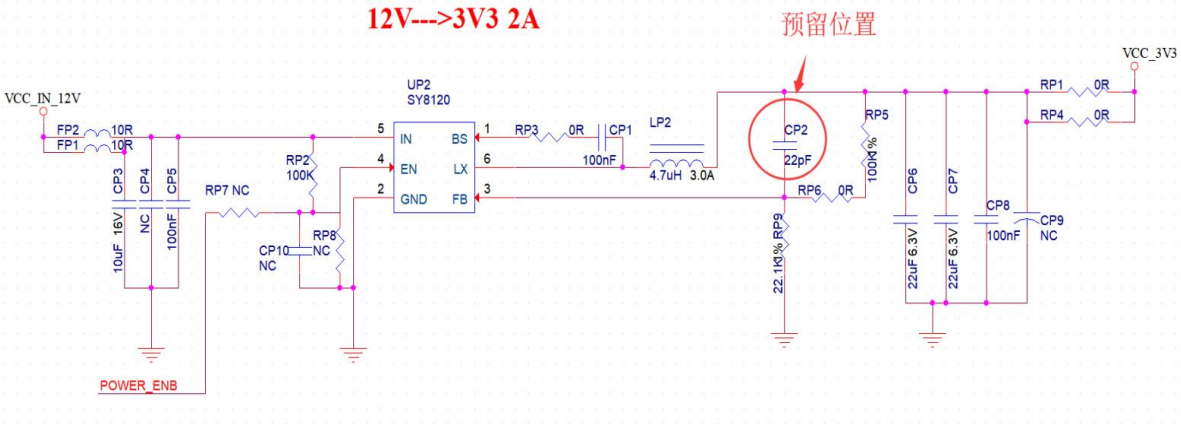


Figure 13 DC-DC step-down circuit diagram

7.5. GPIO

- There are some IO ports on the periphery of the module. If you need to use it, it is recommended to connect a 10-100 ohm resistor in series with the IO ports. This can suppress overshoot and make the levels on both sides more stable. Helpful for both EMI and ESD.
- For the pull-up and pull-down of the special IO port, please refer to the instructions in the specification, which will affect the startup configuration of the module.
- The IO port of the module is 3.3V. If the level of the main control and the IO port of the module do not match, a level conversion circuit needs to be added.
- If the IO port is directly connected to the peripheral interface, or terminals such as pin headers, it is recommended to reserve an ESD device near the IO port wiring near the terminal.

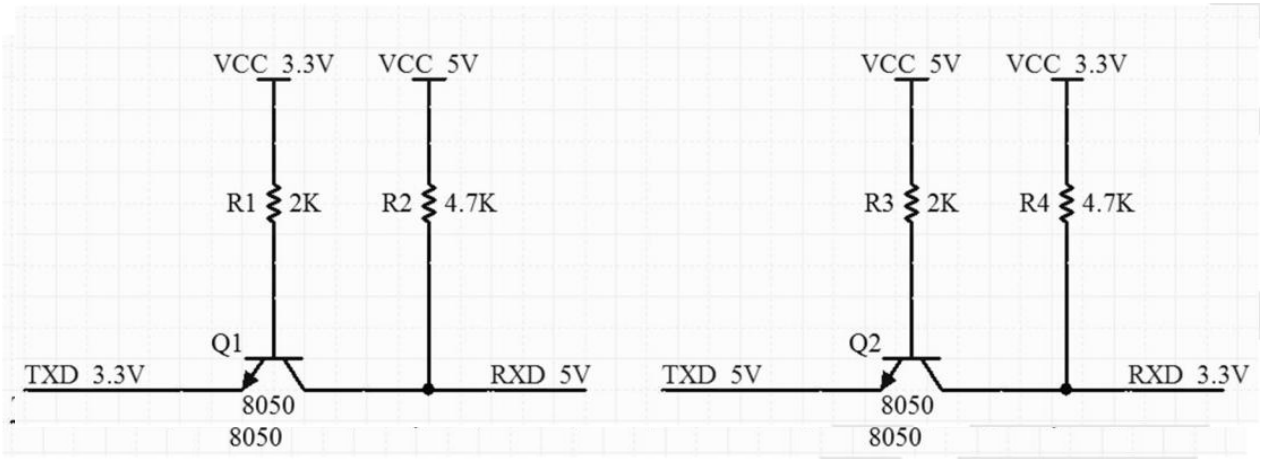


Figure 14 Level convert circuit

8. Storage conditions

Products sealed in moisture-proof bags should be stored in a non-condensing atmosphere at <40° C/90%RH.

The moisture sensitivity level MSL of the module is 3.

After the vacuum bag is unpacked, it must be used within 168 hours at 25±5° C/60%RH, otherwise it needs to be baked before it can be put online again.

9. Reflow welding curve diagram

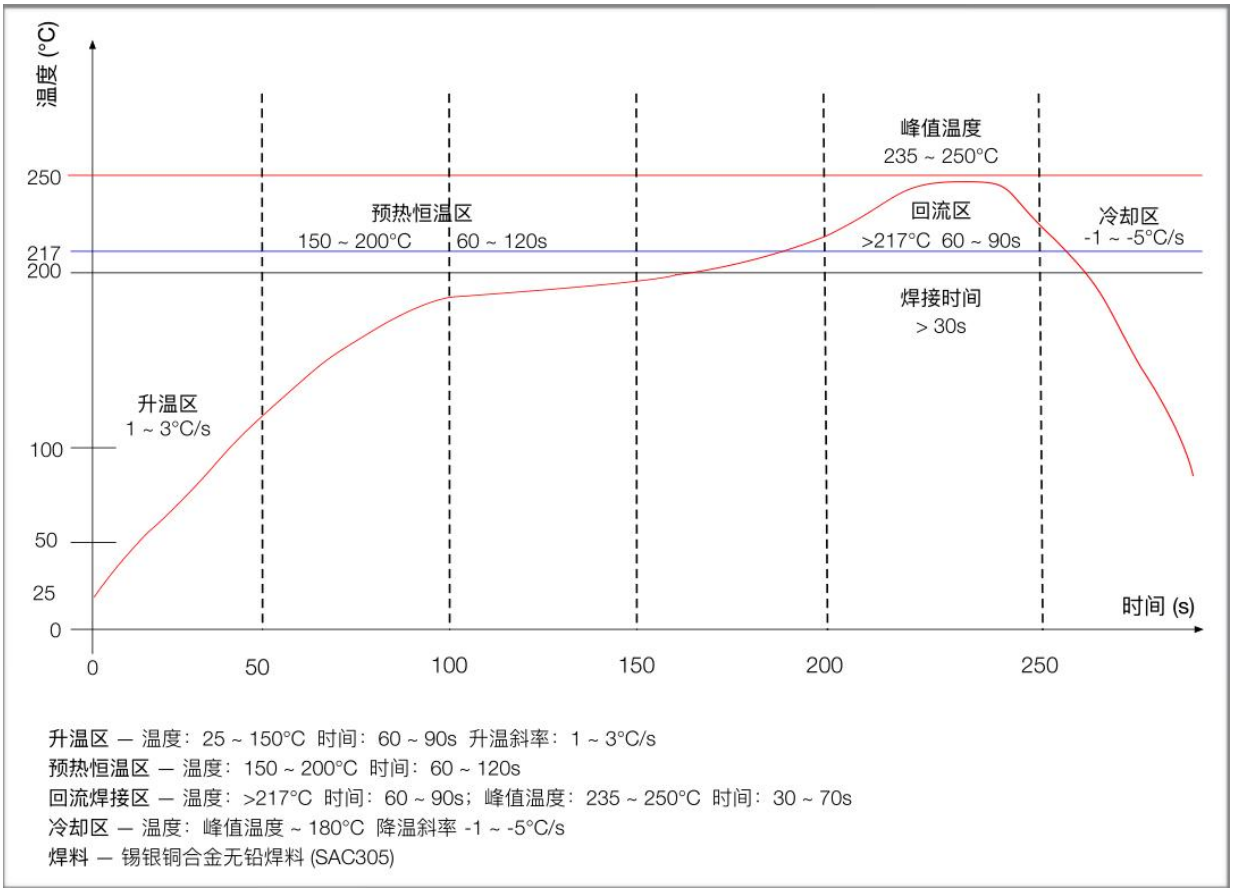


Figure 15 Reflow welding diagram

10.Product Packaging Information

Ai-WB3-12F module was packaged in a tape, 800pcs/reel.As shown in the below image:

Figure 16 Package and packing diagram

11.Contact us

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