BU04 Specification

Version V1.0.0

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Document Resume

Version	Date	Develop/revise content	Edition	Approve
V1.0.0	2024.06.24	First Edition	XiHuan Lv	Ning Guan

Content

1. Product Overview

BU04 is a dual-antenna ultra-wideband (UWB) module designed by Shenzhen Anxinke Technology Co., Ltd. based on Decawave's DW 3000 series chips . BU0 4 integrates DW3000+STM32F103 MCU and supports dual onboard antennas or dual IPEX external antennas. BU0 4 can be used in two-way ranging , TDOA or PDOA positioning systems, with a positioning accuracy of up to 10 cm and supports a data rate of up to 6.8 Mbps. It can be widely used in precise positioning, underground positioning in coal mines, hospital personnel positioning, warehouse positioning, various indoor positioning and other fields.

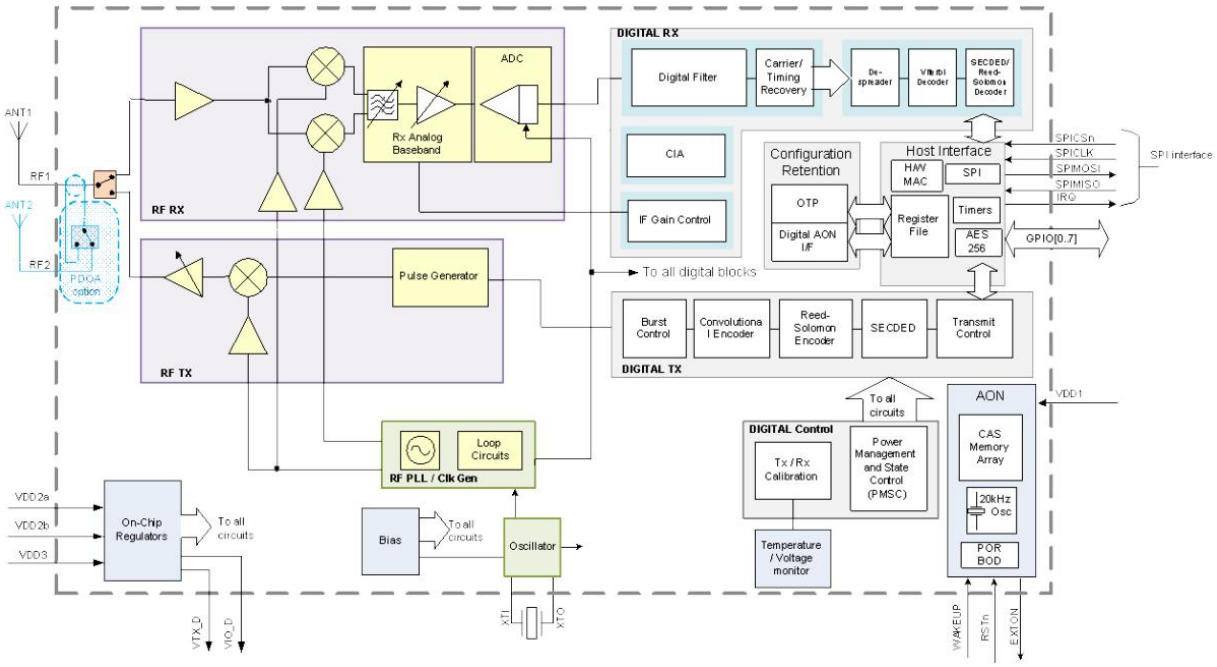


Figure 1 Main chip architecture diagram

1.1. Characteristic

- Adopt SMD-34 package , compatible with DIP-16 package
- Compliant with IEEE 802.15.4-2015 UWB standard
- Compliant with IEEE802.15.4z (BPRF mode)
- Support dual antenna channels
- Support channel 5 and channel 9
- Simple integration, no need for RF secondary design
- Support onboard antenna, compatible with IPEX external antenna
- Integrated MAC function
- Using RTLS infrastructure to extend communication range
- Data rate supports 850 K bps, 6.8 Mbps
- Supports two-way ranging and T DOA and PDOA positioning solutions
- Provide precise positioning and data transmission
- Positioning accuracy 10 cm
- Supports high label density
- Integrated HW AES 256
- Support SPI interface
- 20 configurable GPIOs
- Integrated STM32F103 MCU
- Programmable adjustable transmission power
- Supports supply voltage from 2.5 V to 3.6 V

2. Main parameters

Table 1 Description of main parameters

Model	BU04
Package	SMD-34 compatible with DIP-16
Size	35.5 * 33.5 *3.4(±0.2)mm
Antenna type	Onboard PCB antenna compatible with IPEX socket
Center frequency	CH5 (6489.5MHz), CH9 (7987.2MHz)
Operating temperature	-40℃~ 85℃
Storage Environment	-40℃~ 125℃, < 90%RH
Power supply range	Supply voltage 2.5 V ~ 3.6 V, typical value 3.3 V. Supply current ≥ 500 mA
Supported interfaces	SPI , UART, I2C,
Available IO quantity	20
Built-in MCU	STM32F103

2.1. Static electricity requirements

The BU04 is an electrostatically sensitive device and requires special precautions when handling .

Figure 2 ESD anti-static diagram

2.2. Electrical characteristics

Table 2 Electrical characteristics table

parameter		condition	Minimum	Typical Value	Maximum	unit
Supply voltage		VDD 1	1.7	3. 3	3.6	V
Supply voltage		3V3	2.5	3.3	3.6	V
I/O	VIL	-	-	-	0.3*3V3	V
	VIH	-	0.7*3V3	-	-	V
	VOL	-	-	0.1*3V3	-	V

	VOH	-	-	0.9*3V3	-	V
	IMAX	-	-	-	10	mA

2.3. RF parameters

Table 3 UWB RF parameters

Description	Typical Value	Unit
CH5 center frequency	6489.6	MHz
CH9 center frequency	7987.2	MHz
Channel bandwidth	499.2	MHz

2.4. Power consumption

The following power consumption data is based on a 3.3 V power supply and an ambient temperature of 25°C .

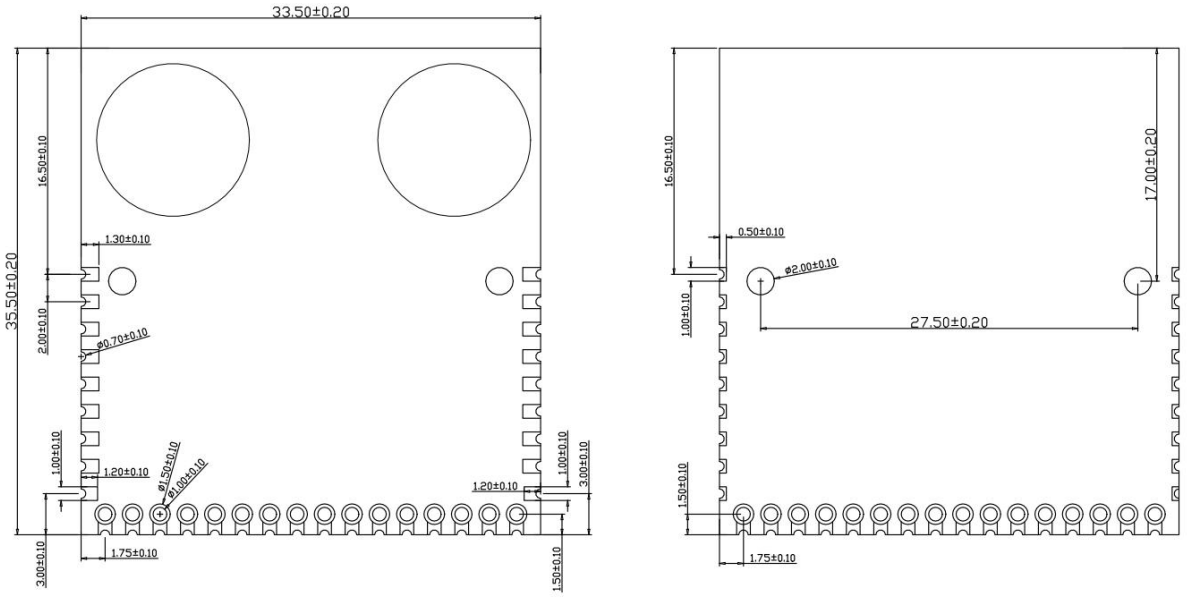
Table 4 Power consumption table

Mode	Min.	Typical value	Max.	Unit
CH5 transmission, rate 0.85Mbps	-	45.39	-	mA
CH5 transmission, rate 6.81Mbps	-	43.19	-	mA
CH9 transmission, rate 0.85Mbps	-	53.18	-	mA
CH9 transmit, rate 6.81Mbps	-	51.16	-	mA
CH5 receiving, rate 0.85Mbps	-	50.83	-	mA
CH5 receiving, rate 6.81Mbps	-	51.19	-	mA
CH9 receiving, rate 0.85Mbps	-	79.28	-	mA
CH9 receiving, rate 6.81Mbps	-	79	-	mA

3. Appearance dimensions

Front Front Back

Figure 3 Appearance of the module(the rendering is for reference only, the actual object shall prevail)

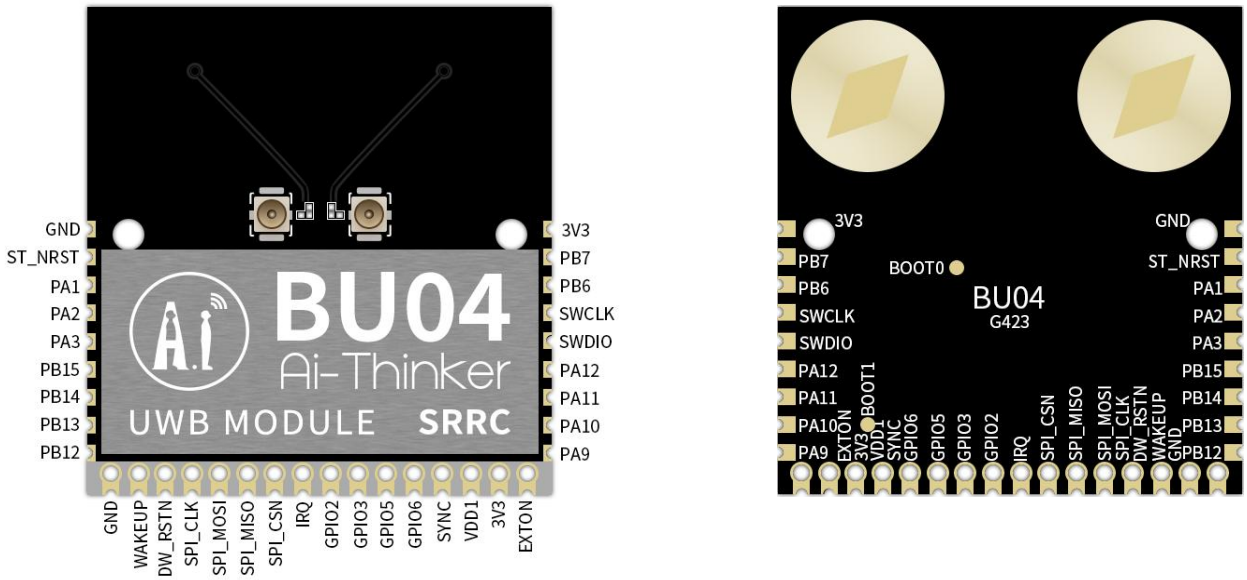


Front Back

Figure 4 Module size diagram

4. Pin Definition

BU04 module has a total of 34 pins , as shown in the pin diagram. The pin function definition table is the interface definition.



Front Back

Figure 5 Pin diagram

Table 5 Pin function definition table

No.	Name	Function	Power domains
1	GND	Grounding	GND
2	ST_NRST	NRST; STM32 reset pin, pull low to be effective	3V3
3	PA1	STM32 PA1;ADC12_IN1/TIM2_CH2	3V3
4	PA2	STM32 PA2;USART2_TX/ADC12_IN2/TIM2_CH3	3V3
5	PA3	STM32 PA3;USART2_RX/ADC12_IN3/TIM2_CH4	3V3
6	PB15	STM32 PB15;SPI2_MOSI/TIM1_CH3N	3V3
7	PB14	STM32 PB14;SPI2_MISO/USART3_RTS/TIM1_CH2N	3V3
8	PB13	STM32 PB13;SPI2_SCK/USART3_CTS/TIM1_CH1N	3V3
9	PB12	STM32 PB12;SPI2_NSS/I2C2_SMBA/USART3_CK/TIM1_BKIN	3V3
10	GND	Grounding	GND

11	WAKEUP	WAKEUP/PB0; DW3000 chip WAKEUP is connected to STM32 PB0. When it is activated high, the WAKEUP pin brings DW3000 from sleep or DEEPSLEEP state to operation mode	3V3
12	DW_RSTN	RSTN/PA0; RSTN of DW3000 chip connected to STM32 PA 0. Valid at low level. Can be pulled low by external open-drain driver to reset DW3000. Must not be pulled high by external power supply. Validating RSTn pin will completely reset the device, equivalent to a power cycle	3V3
13	SPI_CLK	SPI_CLK /PA5; DW3000 chip SPI_CLK is connected to STM32 PA5 . SPI communication clock	3V3
14	SPI_MOSI	SPI_MOSI /PA7; DW3000 chip SPI_MOSI is connected to STM32 PA7 . SPI data input	3V3
15	SPI_MISO	SPI_MISO /PA6; DW3000 chip SPI_MISO is connected to STM32 PA6 . SPI data output	3V3
16	SPI_CSN	SPICSn /PA4 ; DW3000 chip SPICSn connected to STM32 PA 4. SPI chip select. A high-to-low transition on SPICSn signals the start of a new SPI transaction. SPICSn can also be used as a wake-up signal to bring the DW3000 out of SLEEP or DEEPSLEEP state	3V3
17	IRQ	GPIO8/IRQ/PB5; DW3000 chip GPIO8/IRQ is connected to STM32 PB5. General I/O pin. Interrupt request output from DW3000 to the host processor. By default, IRQ is an active high output, but can be configured as low active if necessary. For correct operation in SLEEP and DEEPSLEEP modes, it should be configured as active high active. This pin will float in SLEEP and DEEPSLEEP states and may cause false interrupts on the host unless it is pulled low externally (100kΩ is recommended). When the IRQ function is not used, the pin can be reconfigured as a general I/O line	3V3
18	GPIO2	GPIO2/TXLED; General purpose I/O pin. It can be configured to be used as a RXLED driver pin, which can be used to light up the LED during receive mode	VDD 1
19	GPIO3	GPIO3/TXLED; General purpose I/O pin. It can be configured to be used as a TXLED drive pin, which can be used to light up an LED after transmission	VDD1
20	GPIO5	GPIO5/EXTTXE/SPIPOL; General purpose I/O pin. On power up, it acts as the SPIPOL (SPI polarity select) pin, which is used to configure the SPI mode of operation. After power up, the pin will default to a general purpose I/O pin. It can be configured to function as EXTTXE (External Transmit Enable). This pin goes high when the DW3000 is in transmit mode	VDD1

21	GPIO6	GPIO6/EXTRXE/SPIPHA; General purpose I/O pin. At power up, it acts as the SPIPHA (SPI Phase Select) pin, which is used to configure the SPI mode of operation. It can be configured to act as an EXTRXE (External Receiver Enable). This pin goes high when the DW3000 is in receive mode. After power up, the pin will default to a general purpose I/O pin	VDD1
22	SYNC	GPIO7/SYNC/PB1; DW3000 chip GPIO7/SYNC is connected to STM32 PB1. The SYNC input pin is used for external synchronization. When the SYNC input function is not used, this pin can be reconfigured as a general I/O pin	3V3
23	VDD1	Power supply, 2.5 V ~ 3.6 V , external power supply output current is recommended to be above 500mA	VDD1
24	3V3	Power supply, 2.5 V ~ 3.6 V , external power supply output current is recommended to be above 500mA	3V3
25	EXTON	EXTON /PA8 ; DW3000 chip EXTON is connected to STM32 PA8. External device enabled . Takes effect during wake-up and remains active until the device enters sleep mode. Can be used to control external DC-DC converters or other circuits that are not needed when the device is in sleep mode to minimize power consumption	3V3
26	PA9	STM32 PA9;USART1_TX/TIM1_CH2	3V3
27	PA10	STM32 PA10;USART1_RX/TIM1_CH3	3V3
28	PA11	STM32 PA11;USART1_CTS/CANRX/USBDM/TIM1_CH4	3V3
29	PA12	STM32 PA12;USART1_RTS/CANTX/USBDP/TIM1_ETR	3V3
30	SWDIO	STM32 PA13;JTMS/SWDIO	3V3
31	SWCLK	STM32 PA14;JTCK/SWCLK	3V3
32	PB6	STM32 PB6;IC21_SCL/TIM4_CH1	3V3
33	PB7	STM32 PB7;IC21_SDA/TIM4_CH2	3V3
34	3V3	Power supply, 2.5 V ~ 3.6 V , external power supply output current is recommended to be above 500mA	3V3
Note:It is recommended to lead SWDIO and SWCLK out of the test point to facilitate STM32 programming			

5. Schematic

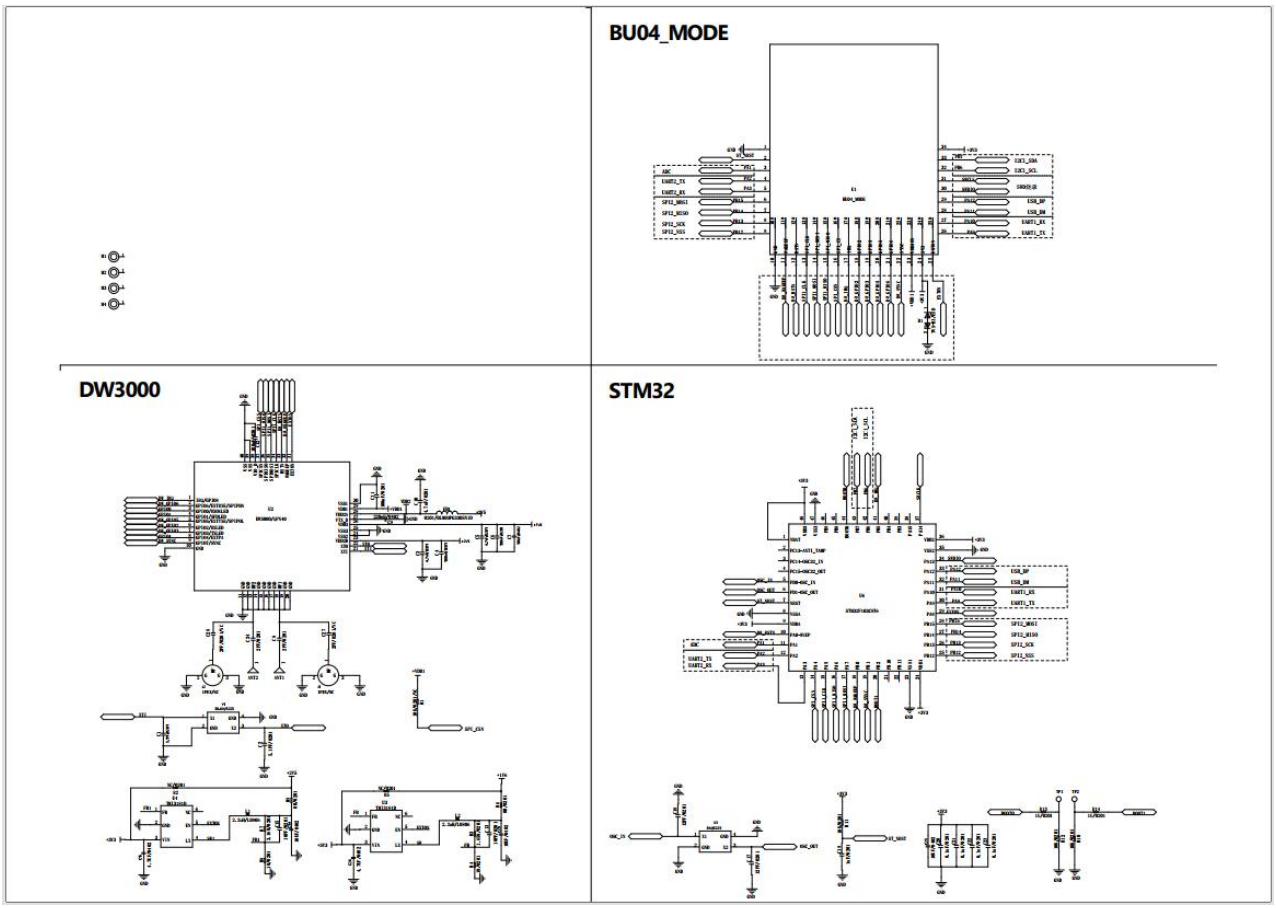


Figure 6 Schematic diagram

6. Antenna parameters

6.1. Antenna test prototype diagram

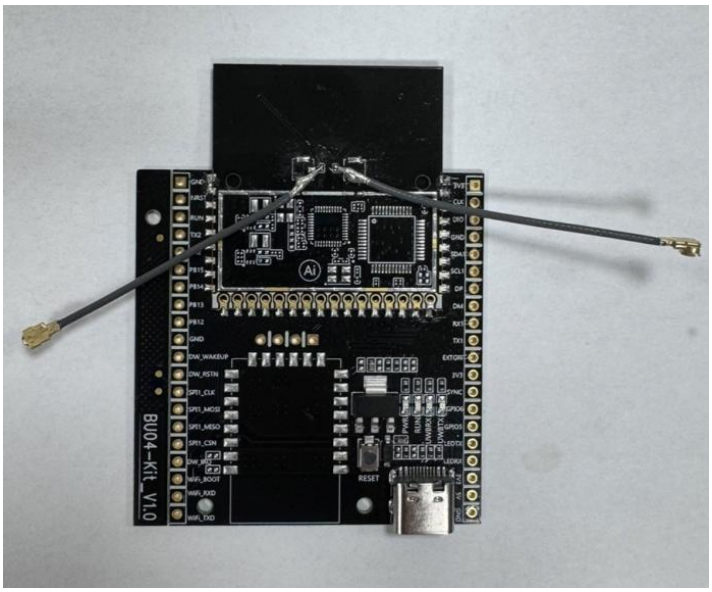


Figure 7 Schematic diagram of antenna test prototype

6.2. Antenna S parameters

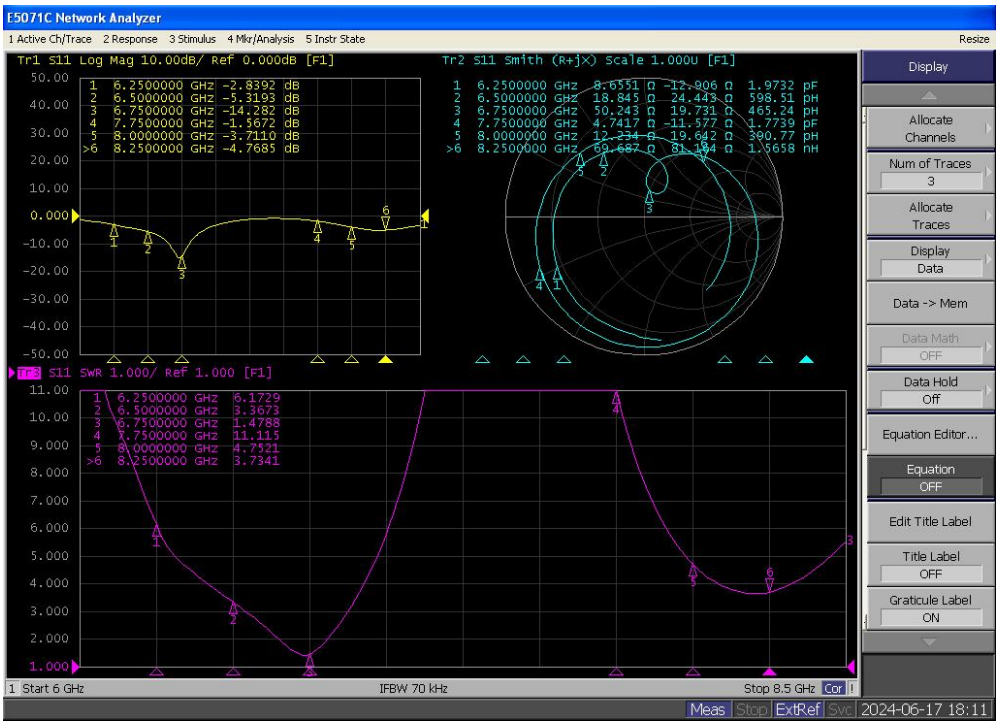


Figure 8 Antenna S parameters (RF 1)

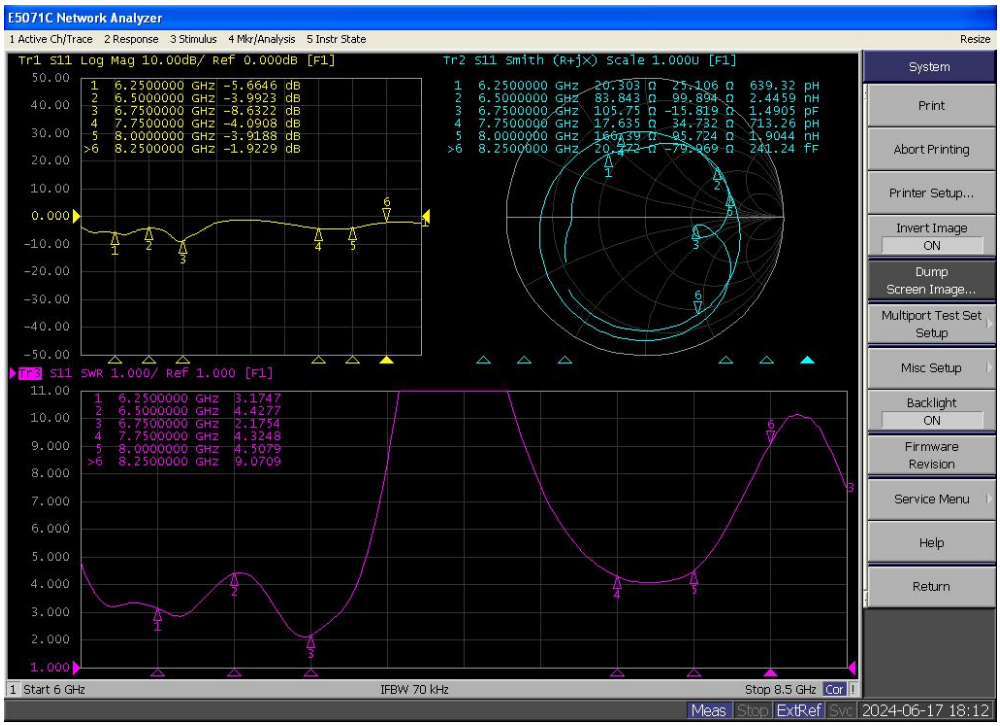


Figure 9 Antenna S parameters (RF2)

6.3. Application Guide Circuit

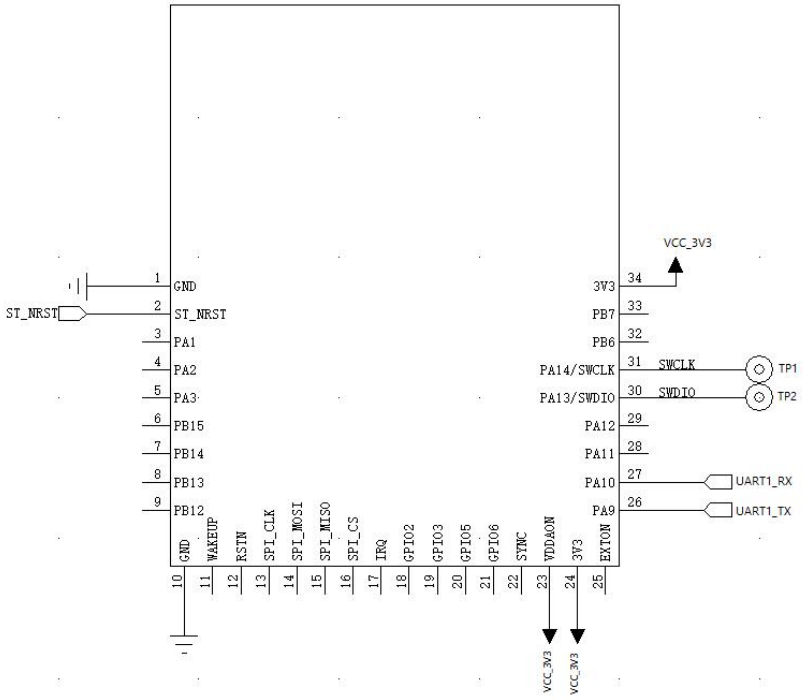


Figure 10 Application guidance circuit

6.4. Recommended PCB package size

- SMD-34

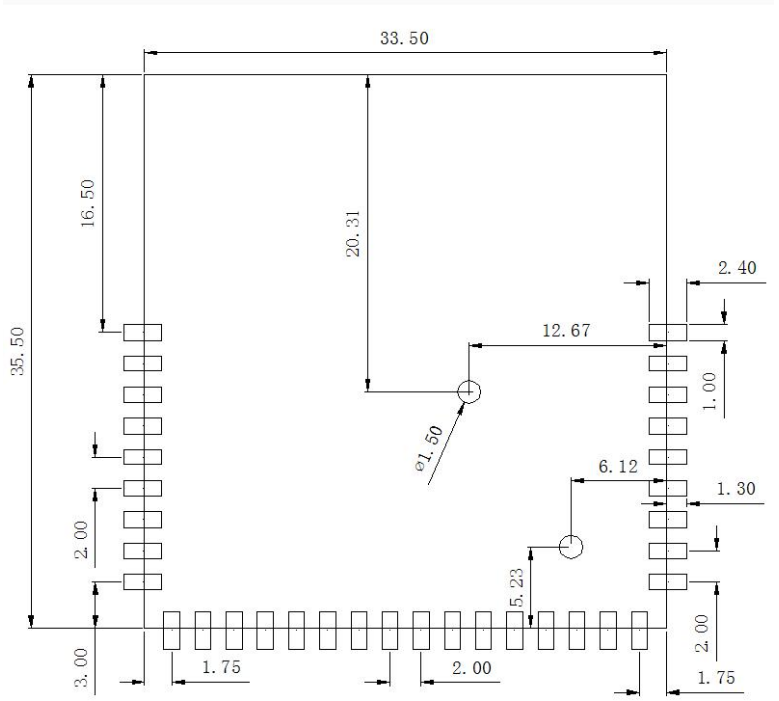


Figure 11 Recommended PCB package size (SMD-34)

- DIP-16

The DIP-16 package is a 2.0mm pitch single-row jack 16P , designed according to the standard 2.0mm single-row pin header

6.5. Antenna layout requirements

- The following two methods are recommended for the installation position on the motherboard:

Solution 1: Place the module on the edge of the motherboard, with the antenna area extending out of the edge of the motherboard.

Solution 2: Place the module on the edge of the main-board and hollow out an area on the edge of the main-board at the antenna position .

- To ensure the performance of the onboard antenna, metal parts must not be placed around the antenna and must be kept away from high-frequency devices.

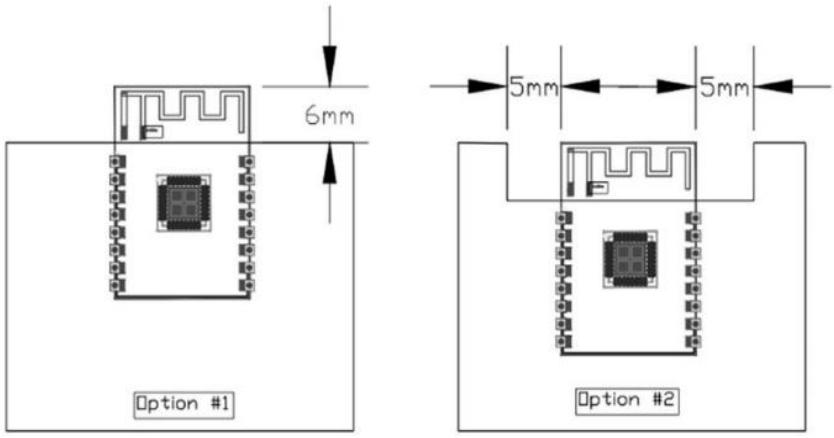


Figure 12 Schematic diagram of antenna layout

6.6. powered by

- The recommended voltage is 3.3V and the peak current is above 500mA .
- It is recommended to use LDO power supply; if DC-DC is used, it is recommended to control the ripple within 30mV.
- It is recommended to reserve space for dynamic response capacitors in the DC-DC power supply circuit to optimize the output ripple when the load changes greatly.
- It is recommended to add ESD devices to the 3.3V power interface.

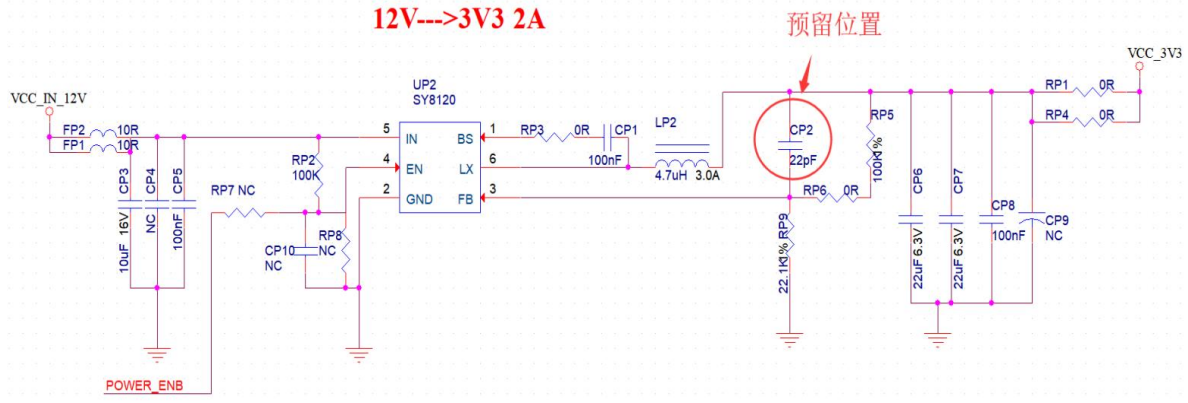


Figure 13 DC-DC buck circuit diagram

6.7. GPIO

- Some IO ports are connected to the module. If you need to use them, it is recommended to connect a 10-100 ohm resistor in series to the IO ports. This can suppress overshoot and make the levels on both sides more stable. It is helpful for EMI and ESD.
- For the pull-up and pull-down of special IO ports, please refer to the instructions in the

specification, which will affect the startup configuration of the module.

- The IO port of the module is 3.3V. If the IO port levels of the main control and the module do not match, a level conversion circuit needs to be added.
- If the IO port is directly connected to a peripheral interface, or a pin header or other terminal, it is recommended to reserve ESD devices near the terminals in the IO port routing.

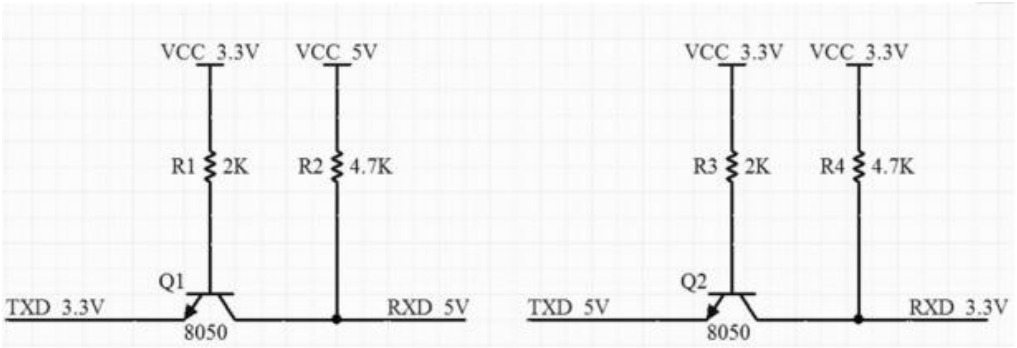


Figure 14 Level conversion circuit

7. Storage conditions

Products sealed in moisture-proof bags should be stored in a non-condensing atmosphere of <40° C/90%RH.

The module's moisture sensitivity level MSL is level 3.

After the vacuum bag is unsealed, it must be used within 168 hours at 25±5℃/60%RH, otherwise it needs to be baked before it can be put online again.

8. Reflow Oven Profile

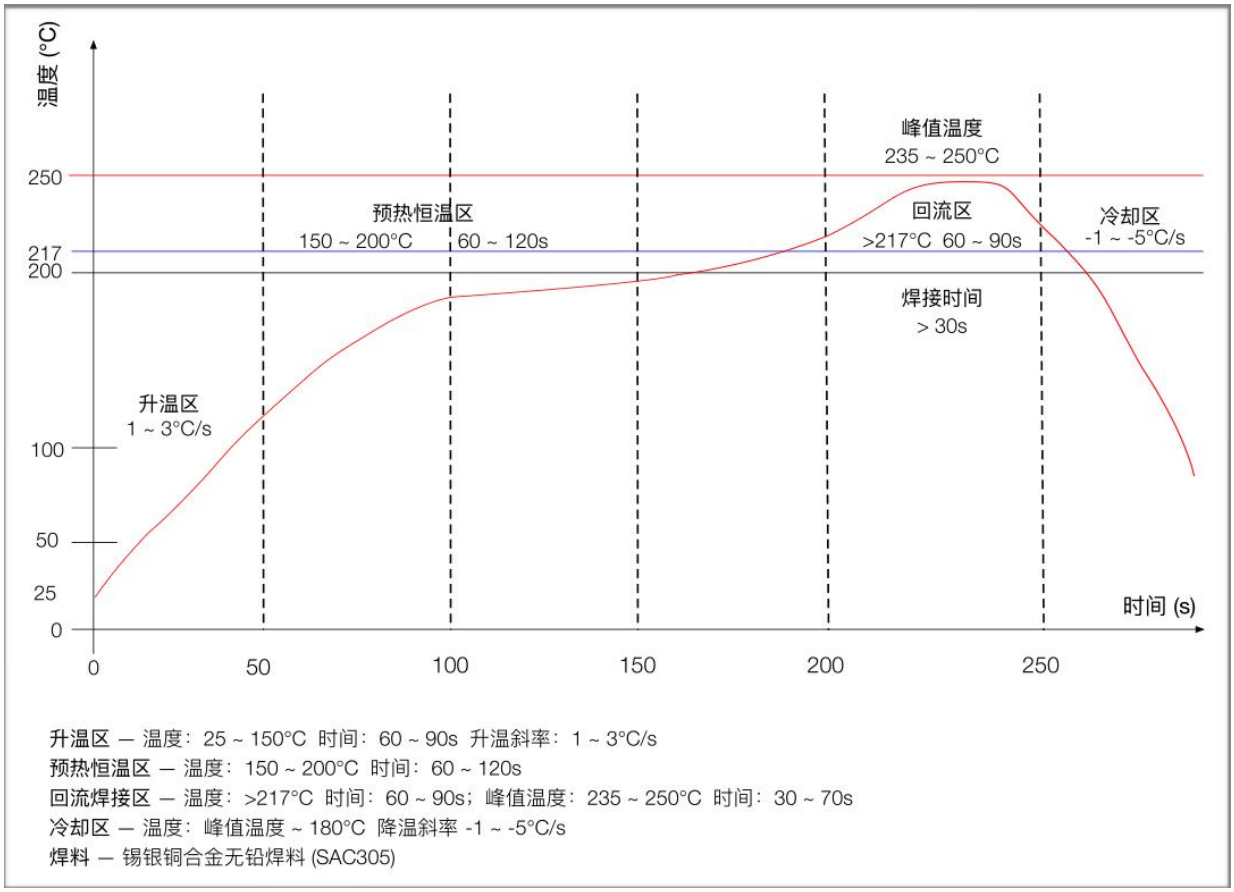


Figure 15 Reflow Oven Profile

9. Product packaging information

BU04 module adopts braid packaging, 350pcs/ disk. As shown in the picture below:

Figure 16 Packaging Taping Diagram

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