Rd-04 Module Manual

Version V1.0.0

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Document resume

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Content

1. Module Introduction

Rd-04 is a motion sensing module based on X-band radar developed by Shenzhen Ai-Thinker Technology Co., LTD. The module uses a Phosense XBR818 chip with a center frequency of 10.525GHz. The module design adopts fixed frequency, directional transmitting and receiving antenna (1T1R), integrates the functions of medium frequency demodulation, signal amplification and digital processing, and has the ability of delay setting and adjustable perception range. The module has the advantages of no wall penetration, anti-interference, small size, good suppression effect of clutter and high harmonic, high stability and consistency. In the module pulse power supply mode, the power consumption is in the micro-ampere level. The module is mainly aimed at low-cost and low-power consumption applications.

The module is suitable for embedded concealed installation, not affected by temperature / humidity, lampblack, water mist, etc., can be widely used in all kinds of lamps, such as bulb lamp, downlight, ceiling light, etc.; low power application scenarios, such as visual doorbell, cat eye, door lock, low power camera, intelligent litter box, feeder, etc.

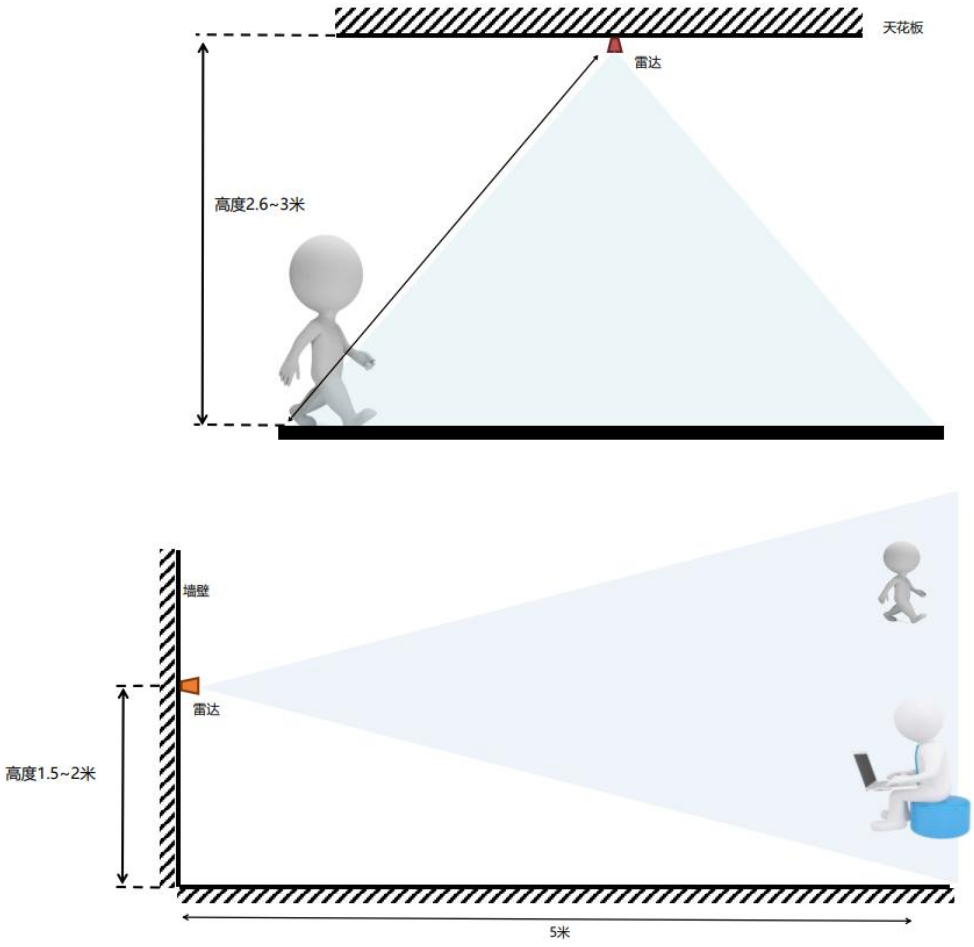


Figure 1 Rd-04 use method

2. Module features and solution advantages

2.1. Module features

- DIP package with standard 2.0mm pin header
- The radar supports the 10.525G frequency
- Integrated digital signal detection and processor, motion target detection results in real-time output
- Support for the IIC bus configuration
- Support the pulse power supply mode
- Support for integrated photosensitive drive
- Support top-hanging, wall-hanging and other installation methods
- The longest radar induction range is up to 6.5 meters
- The radar detection angle is large, and the coverage range can reach ±50degrees

2.2. Solutions advantage

The Rd-04 module uses 10.525GHz radar sensor technology, which is mainly designed for low-cost and low-power consumption applications, and has obvious advantages compared with other solutions:

1. In addition to the movement of the human body induction sensitive, for the traditional scheme can not identify the micro-moving human body can also be sensitive induction;
2. Have good environmental adaptability, the induction effect is not affected by the temperature, humidity, lampblack and water fog and other surrounding environment;
3. Support regular power supply mode and adjustable duty cycle low power consumption mode, with current as low as 110 μ A in pulse power supply mode;
4. Good stability and consistency;

3. Application

- **Smart Home:**

Sensing the presence and distance of the human body and reporting the monitoring results, the appliances can be intelligently controlled to operate on demand;

- **Smart Security:**

Sensor access control, sensor alarms, trigger linkage applications with cameras, etc.

- **Smart switches, lighting, recognizing and sensing the human body:**

Public place or home lighting equipment such as hand-swept switches (hotel, home panel switches, 86 control boxes)

4. Hardware instruction

4.1. Appearance size

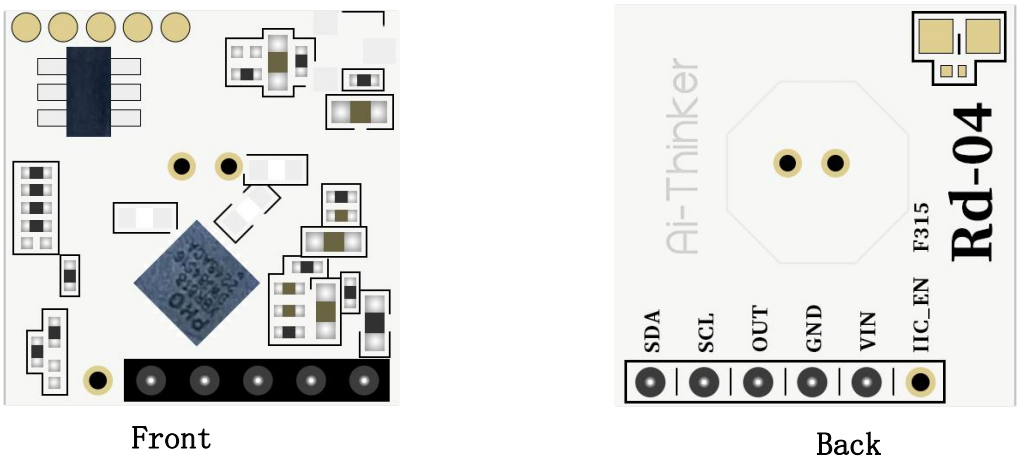


Figure 2 Appearance diagram（The rendering is for reference only, subject to the physical object）

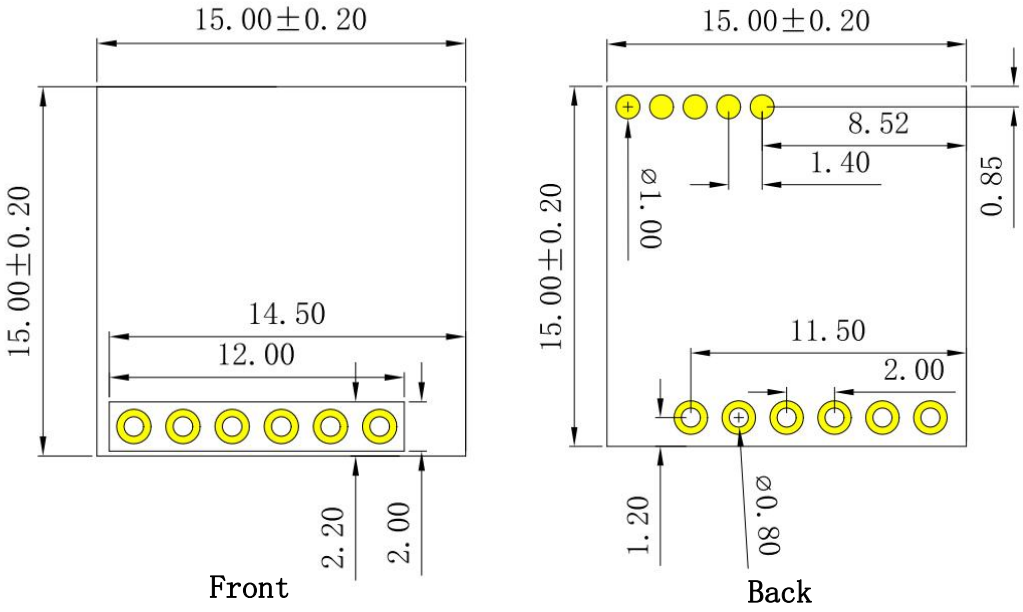


Figure 3 Size diagram

4.2. Pin definition

The Rd-04 module is connected with 6 pins, such as the schematic diagram of the pin, and the pin function definition table is the interface definition.

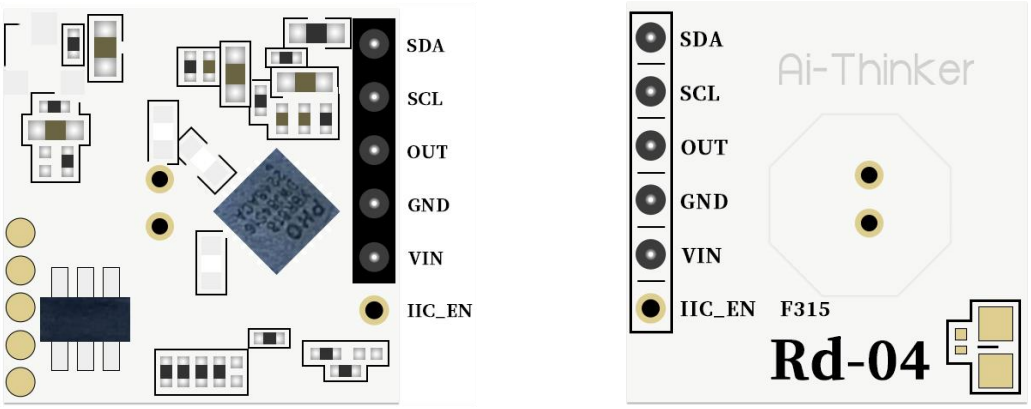


Figure 4 Schematic diagram of the pin

Table 1 Definition table of pin function

No.	Name	Function
1	SDA	IIC SDA
2	SCL	IIC SCL
3	OUT	Detection result output, output high level when sensing, output low level when not sensing
4	GND	Ground
5	VIN	3.3V power input
6	IIC_EN	IIC enables, when you configure Rd-04 with an external MCU, this pin need connect to the IO port of the external MCU for low power consumption

5. Function introduction and reference design

5.1. Function introduce

5.1.1. Pressure control shock block

Provide the 10.525G clock frequency for the entire chip, which the radar also works on, to control the frequency of the VCO through the external ADC1 PIN and the internal register 0x02 [7:4]

5.1.2. PA function block

The power amplification module can amplify the clock signal from the VCO to the required power size, and finally transmit it through the TX pin and antenna. The size of the PA output power can be adjusted by 0x03 [2:0].

5.1.3. LNA function block

The low-noise amplification module can amplify the weak signal of the receiving antenna to a certain range, achieve a certain signal-to-noise ratio index, and meet the application requirements of the post-stage circuit

5.1.4. MIXER function block

The mixer module can output the IF signal from the radio frequency echo signal frequency received by the RX and the VCO frequency mixing operation to the rear circuit.

5.1.5. IF（OP）function block

The transport and release module can adjust the gain of transport and discharge through the off-chip resistance. After the IF signal is amplified and bandwidth limited by operation and discharge, the IF signal that meets the demand is sent to the next level for processing.

5.1.6. PGA&ADC function block

The PGA module in the chip is between IF input and ADC, amplifying the input signal. bypass PGA or different magnification can be selected through the register configuration. The ADC module can reach a sampling rate of 1Mbps, and relevant parameters can be modified by register to convert IF signal into digital signal for target detection.

5.1.7. OSC16M/OSC32K function block

The internal high-precision clock oscillation circuit provides the working clock to the digital module. There are two clocks, respectively 16 MHz and 32 KHz, which can adjust the output frequency through registers, and different chips have certain differences.

5.1.8. BB function block

The functional module integrates the algorithm of mobile target detection. Through the register configuration, different parameters can be set to complete the detection of the moving target and generate the corresponding trigger signal.

5.1.9. BG/LDO12/RFLDO function block

The internal power supply module of the chip converts the input 3.3V voltage into the 1.2V voltage required for the operation of each internal function module.

5.2. Reference design

5.2.1. The relation between resistance value of ADC 1 and VCO frequency

Table 2 The VCO frequency configuration

Level	ADC value	Best setting value	External resistance value（ADC ref set to 3V)	VCO frequency
1	0~255	127	18K_1%	？Wait for test
2	256~511	383	56K_1%	？Wait for test
3	512~767	639	93.1K_1%	？Wait for test
4	768~1023	895	130K_1%	？Wait for test
5	1024~1279	1151	169K_1%	？Wait for test
6	1280~1535	1407	205K_1%	？Wait for test
7	1536~1791	1663	243K_1%	？Wait for test
8	1792~2047	1919	280K_1%	？Wait for test
9	2048~2303	2175	316K_1%	？Wait for test
10	2304~2559	2431	357K_1%	？Wait for test
11	2560~2815	2687	390K_1%	？Wait for test

12	2816~3071	2943	430K_1%	？Wait for test
13	3072~3327	3199	470K_1%	？Wait for test
14	3328~3583	3455	510K_1%	？Wait for test
15	3584~3839	3711	549K_1%	？Wait for test
16	3840~4095	3967	576K_1%	？Wait for test

The VCO frequency is divided into 16 levels, and the corresponding resistance value of each gear is calculated as follows:

R=[1/32+(n-1)/16] x adc_ref /5uA

5.2.2. The relationship between the resistance value of the ADC 2 external configuraion and the BB threshold gate

Table 3 BB Module Threshold Configuration

Level	ADC value	Best setting value	External resistance value（ADC ref set to 3V)	Threshold value
1	0~255	127	18K_1%	0x0040
2	256~511	383	56K_1%	0x0060
3	512~767	639	93.1K_1%	0x0080
4	768~1023	895	130K_1%	0x00A0
5	1024~1279	1151	169K_1%	0x00C0
6	1280~1535	1407	205K_1%	0x0100
7	1536~1791	1663	243K_1%	0x0180
8	1792~2047	1919	280K_1%	0x0200
9	2048~2303	2175	316K_1%	0x0300
10	2304~2559	2431	357K_1%	0x0400
11	2560~2815	2687	390K_1%	0x0500
12	2816~3071	2943	430K_1%	0x0600
13	3072~3327	3199	470K_1%	0x0800
14	3328~3583	3455	510K_1%	0x0A00
15	3584~3839	3711	549K_1%	0x0C00
16	3840~4095	3967	576K_1%	0x1000

The BB threshold is divided into 16 levels, and the corresponding resistance value of each

threshould is calculated as follows:

R=[1/32+(n-1)/16] x adc_ref /5uA

5.2.3. The relation between the resistance value of the external configuration of ADC 3 and the BB delay time

Table 4 Late time configuration of the BB module

Level	ADC value	Best setting value	External resistance value（ADC ref set to 3V)	Delay time
1	0~255	127	18K_1%	5s
2	256~511	383	56K_1%	10s
3	512~767	639	93.1K_1%	15s
4	768~1023	895	130K_1%	20s
5	1024~1279	1151	169K_1%	30s
6	1280~1535	1407	205K_1%	45s
7	1536~1791	1663	243K_1%	60s
8	1792~2047	1919	280K_1%	120s
9	2048~2303	2175	316K_1%	180s
10	2304~2559	2431	357K_1%	240s
11	2560~2815	2687	390K_1%	300s
12	2816~3071	2943	430K_1%	600s
13	3072~3327	3199	470K_1%	900s
14	3328~3583	3455	510K_1%	1200s
15	3584~3839	3711	549K_1%	1800s
16	3840~4095	3967	576K_1%	3600s

The BB delay time is divided into 16 stages, and the corresponding resistance value of each gear is calculated as follows：

R=[1/32+(n-1)/16] x adc_ref /5uA

6. Register description and schematic diagram

XBR818's IIC Device ID=7'h71

Receive timing for one byte:

S	DEVID[6:0]	Wn	A	DATA	A	P

Receive timing for sequential transmission:

S	DEVID[6:0]	Wn	A	Reg_Addr	A	DATA0	A	……	DATAn	A	P

Transmit timing:

S	DEVID[6:0]	R	A	DATA0	A	……	DATAn	A	P

6.1. LDO_DIG/RFLDO function register

0x1	b'10	R/W	ldo_dig_trim	[4:3]	1.2V ldo trim

LDO_DIG register：

Can fine-tune the internal digital part of the 1.2 VLDO voltage, a total of 4 levels is adjustable, the default value isb‘10;

0x2	b'1	R/W	rf1_en	[3]	rf ldo1 enable
	b'000	R/W	rfldo1_trim	[2:0]	rf ldo1 trim

0x4	b'0	R/W	rf_en_sel	[7]	rf ldo enable select 0:adc sample enable ldo 1:by reg rfx_en12 setting

RFLDO register：

RFLDO can be switched through BIT [3] of 0x2, the voltage output of RFLDO can be fine-tuned through 0x2 BIT [2:0], a total of 8 adjustable, the default value is b‘000; 0x4 BIT [7]

can choose to use ADC Sample signal to enable RFLDO, realize pulse power supply, or regular power supply;

6.2. OSC16M/OSC32K function register

0x0	0x48	R/W	osc16m_trim	[7:0]	rc osc frequency trim

bit【7：0】is to adjust the internal 16 MHz frequency, a total of 8 bits to set, can adjust the frequency from about 7 MHz to about 26 MHz;

0x6	0x52	R/W	osc32k_trim	[6:0]	rc osc32k frequency trim

is to adjust the internal 32 KHz frequency, a total of 7 bits to set, can adjust the frequency from about 22 KHz to about 160 KHz;

6.3. PGA function register

0x7	0x5B	R/W	pga_en	[7]	PGA enable
			pga_bypass	[6]	PGA bypass
			pga_dc_trim	[5:0]	PGA output dc level setting

bit【7】：PGA function switch enable bit，1 enable，0 turn off;

bit【6】：PGA bypass turn on or off enable bit，1 bypass PGA;

bit【5：0】：PGA output DC level adjustment bit, a total of 6 bits to adjust, according to the different PGA input signal, adjust the DC level output of PGA to meet the application requirements;

0xB	b‘010	R/W	pga_gain	[2:0]	PGA gain control(0~7 x1/x1.5/x2/x3/x4/x6/x8/x12)

bit【2：0】：PGA magnification of the control bits, a total of 8 gears can be adjusted, the default value is x2;

6.4. ADC function register

0x8	0xA8	R/W	adc_clk_sel	[7]	adc clock select, 0-> from digital clk, 1-> analog osc16m
			adc_clk_div	[6]	adc clock divide from analog clk
			adc_data_clrn	[5]	adc date clear, 0 ->clear

			adc_mode	[4]	adc mode, 0-> trigger mode, 1-> continues sample mode
			adc_en	[3]	ADC enable
			adc_ch_mux	[2:0]	adc input channel select

bit【7】: ADC circuit clock select bit;

bit【6】: ADC circuit clock IF select bit;

bit【5】: ADC data clear switch bit;

bit【4】: ADC operation mode select bit, 0 is trigger mode, 1 is the continuous sampling mode;

bit【3】: ADC circuit switch enable bit, 1 is for turn on ADC;

bit【2:0】: ADC Input channel selection bits, ADC0: IF; ADC1-ADC3:ananlog; ADC5: VDD/2; ADC6:VCM; ADC7: pluse;

0x9	0x86	R/W	adc_vref_trim	[7:4]	adc reference trim
			adc_vcm_trim	[3:2]	adc vcom trim
			adc_vref_sel	[1:0]	adc reference select, 00->2.5V, 01->2.8V, 10->3.0V, 11->VDD

bit【7: 4】: ADC ref Voltage fine tuning bit, can adjust the accuracy of ref voltage, a total of 8 levels adjustable;

bit【3: 2】: ADC vcom Voltage fine tuning bit, can adjust the accuracy of vcom voltage, a total of 4 levels adjustable;

bit【1: 0】: ADC ref Voltage gear selection bit, a total of 4 gears can be selected;

0xA	0x30	R/W	adc_sample_cnt	[7:0]	adc sample time

bit【7: 0】: The setting bit of ADC sampling pulse width can not be set too small, and determine the pulse power supply pulse width together with RF _ DELAY;

0x5	0x80	R/W	adc_save_pow	[7]	power down after adc_done
				[6:0]	Reserved

bit【7】: Turn off the function after ADC sampling, in order to save power consumption, 1 to enable this function;

0xB	b'010	R/W	adc_vinbais_enb	[6]	disable adc input 5u bias (0->5uA bias enable),ADC1,ADC2,ADC3

bit【6】: For ADC 1, ADC 2, ADC 3, provide 5 uA bias current switching enabling level, 0 enabling open, need to be in the ADC 1, ADC 2, ADC 3 pin external resistance to the ground;

6.5. Set the pulse width for the pulse power supply

0x4	0x20	R/W	rf1_delay	[6:0]	rf ldo1 startup delay
0xA	0x30	R/W	adc_sample_cnt	[7:0]	adc sample time

The pulse width is determined by setting the values of 0x4 register and 0xA register; 0x4 is the RFLDO on output delay, which means that the adc takes a delay to truly open the LDO, ensuring that the ADC is ready. Affect the pulse width, specifically, power supply pulse width = adc_sample_cnt-rf_delay;

6.6. VCO frequency adjust register

0x2	0x88	R/W	vco_cnt	[7:4]	vco frequency tune

bit【7：4】is to fine-tune the RF VCO 10.525GHz frequency, there are 4 bits to set, total16 gears;

6.7. RF transmission power adjust register

0x3	b’101	R/W	vco_sw	[2:0]	rf out power control

bit【2：0】is to adjust the transmitting power of the RF PA, there are 3 bits to set, a total of 8 gears;

6.8. IF output DC point level fine register

0x3	b’100	R/W	mix_swdc	[6:4]	mixer dc trim

bit【6：4】is the level of the IF DC point, there are 3 bits to set, total8 level;

6.9. Photosensitive induction register

0xB	b‘10	R/W	ls_trim	[5:4]	light sensor threshold setting
	b‘1		ls_rstn	[3]	light sensor reset_n

bit【5:4】 is the setting of the photosensitive sensing threshold, which is used in conjunction with the external photosensitive circuit; there are 3 steps in total, and the adjustment range is between 700mV and 1000mV;

bit【3】 is the reset signal for photosensitive sensing, and 0 is the reset state;

6.10.BB module (target detection) function adjustment registers

6.10.1. Setting the ADC sampling frequency

0x10	0x20	R/W	bb_ctl[7:0]	[7:0]	sample rate divider,minimum 2

bit[7:0] configure ADC sampling rate, also pulse frequency of pulse supply, 32KHz OSC clock division, minimum 2, default set to 1KHz

6.10.2. Setting a judgment threshold for the presence or absence of a moving target

0x18	0x0	R/W	bb_thresh1[7:0]	[7:0]	threshold for ac detection
0x19	0x1	R/W	bb_thresh1[15:8]	[7:0]	threshold for ac detection

Bit [15:0] set the target to move with or without discrimination threshold, AC error value exceeding this threshold flag set up

6.10.3. Setting the Noise Update Allowable Threshold

0x1A	0x0	R/W	bb_thresh2[7:0]	[7:0]	threshold for noise detection
0x1B	0x8	R/W	bb_thresh2[15:8]	[7:0]	threshold for nosie detection

Bit [15:0] sets the noise update allowable threshold, the AC error does not exceed this threshold to allow the noise update to be started.

6.10.4. Setting the sensing delay time and lockout time

0x1D	0x0	R/W	t1_value[7:0]	[7:0]	t1 value, io output high cnt @32KHz
0x1E	0xA6	R/W	t1_value[15:8]	[7:0]	t1 value, io output high cnt @32KHz
0x1F	0xE	R/W	t1_value[23:16]	[7:0]	t1 value, io output high cnt @32KHz
0x20	0x0	R/W	t2_value[7:0]	[7:0]	t2 value, io output low cnt @32KHz
0x21	0xFA	R/W	t2_value[15:8]	[7:0]	t2 value, io output low cnt @32KHz
0x22	0x0	R/W	t2_value[23:16]	[7:0]	t2 value, io output low cnt @32KHz

t1_value【23：0】 set the sensing delay time, 24 bits in total. calculation: t1_value = time to be set (unit is s) x 32000, then convert to hexadecimal to fill in the register, the default value is 30s;

t2_value【23:0】set the lock time, 24 bits in total. calculation: t2_value=the time to be set (unit is s)x32000, then convert to hexadecimal to fill in the register, the default value is 2s;

6.10.5. The CPU sets the DC value and Noise value.

0x14	0x0	R/W	bb_dc_init[7:0]	[7:0]	dc initial value for manual mode
0x15	0x80	R/W	bb_dc_init[15:8]	[7:0]	dc initial value for manual mode
0x16	0x0	R/W	bb_ac_init[7:0]	[7:0]	nosie initial value for manual mode
0x17	0x1	R/W	bb_ac_init[15:8]	[7:0]	noise initial value for manual mode

bb_dc_init [15:0] manually sets the DC Value, a total of 16 bits, which is used when choosing not to use dynamic automatic update of the DC Value;

bb_ac_init [15:0] manually sets the noise Value, 16 bits in total, which is used when choosing not to use dynamic automatic update of the noise Value;

6.10.6. Other registers that can be set by BB module

0x11	0x13	R/W	bb_ctl[15:8]	[7]	noise detect low threshold 0:1/4 bb_thresh2 1:1/2 bb_thresh2
				[6:4]	total sum samples setting 0:1x128 1:2x128 2:4x128 3:8x128 4:16x128 others:32x128
				[3:2]	dc average dynamic caculate time select 00:4 cycle 01:8 cycle 10:16 cycle 11:32 cycle
				[1:0]	dc average initial caculate time select 00:4 cycle 01:8 cycle 10:16 cycle 11:32 cycle

bit【7】: Noise detection over threshold detection threshold setting

bit [6:4]: points period configuration, the parameter configuration points, equivalent to the points duration

bit [3:2]: working stage DC average calculation time configuration, unit time is one integration cycle

bit[1:0]: initialization stage DC average calculation time configuration, unit time is one integration cycle

0x12	0x11	R/W	bb_ctl[23:0]	[7]	noise value select 0:auto detect 1:cpu force
				[6]	dc value select 0:auto detect 1:cpu force
				[5:4]	noise variation threshold 00:1/2 01:1/4 10:1/8 11:1/16
				[3:2]	nosie update select 00:1/2 01:1/4 10:1/8 11:1/16
				[1:0]	dc update select 00:1/2 01:1/4 10:1/8 11:1/16

bit【7】: Selection of nosie value for discrimination, automatic detection method or CPU fixed configuration method.

bit【6】: Selection of DC value for discrimination, automatic detection method or CPU fixed configuration method.

bit【5:4】: noise fluctuation range, when the average value of AC is detected to be larger, but the fluctuation is within the setting range, it is still judged as effective noise.

bit【3:2】: Noise computed values update weight configurations that affect the smoothness of the noise values

bit【1:0】: the DC average calculated value updates the weight configuration and affects the smoothness of the DC value

0x13	0x1	R/W	bb_ctl[31:24]	[7]	I2C read only data update enable for 0x26~0x29
				[6:5]	Reserved
				[4]	bb proc threshold mode 0:auto by configure pin 1:manual by cpu control register
				[3]	bb read only data update enable
				[2:1]	read only data select 00:det_dc_sum 01:det_ac_sum 10:det_dc_used 11:det_noise

				[0]	bb proc enable 1:enable

bit [7]: data update enable bit of I2C read-only registers 0x26~0x29

bit [4]: Signal detection threshold selection, external pin selection of gear mode and CPU hosting control mode

bit [3]: data update enable bit for bb read-only registers 0x28, 0x29

bit[2:1]: bb read-only register data selection

bit [0]: signal detection enable, need to configure other parameters before setting 0, and then set 1, due to the signal detection part of the operating clock is 32KHz, switch the bit when the CPU needs to ensure that the length of time enough!

6.11. Other Function Registers

0x1C	0x13	R/W	io_timer_ctl	[7:6]	Reserved
				[5]	t1 value select 0: configure by pin 1:configure by CPU register
				[4:3]	timer interrupt output select 00:1 Second 01:1 Minute 10:1 hour 11:1 day
				[2:1]	light sensor triger timer select 00:disable timer 01:4 Second 10:1 Minute 11:1 hour
				[0]	s/m/h/d counter enable

bit【5】: Sensing delay time setting mode selection, external pin selection gear mode or CPU register control mode

bit【4:3】: Timing interrupt time slot selection

bit【2:1】: Photosensitive detection cycle setting

bit【0】: 32bit timer enable, using 32K clock.

0x23	0x0	R/W	pin_ctl[7:0]	[7:4]	INT_IRQ pin output select 0x0:t3_int_irq 0x1:adc_sample_irq 0x2:adc_accu_irq 0x3:adc_triger 0x4:adc_sample ox5:adc_done 0x6:light_trig 0x7:light_latch 0x8:light_flag 0x9:io_value_out 0xa:io_value_out inverted 0xb: io_value & light_flag 0xc io_value_out & light_flag inverted :pin_ctl[11]
				[3:0]	IO_VAL pin output select 0x0:io_value_out & light_flag 0x1:osc_16m 0x2:osc_32k 0x3:light_trig 0x4:light_latch ox5:light_flag 0x6:adc_triger 0x7:adc_sample 0x8:adc_done 0x9:adc_sample_irq 0xa:adc_accu_irq 0xb: t3_int_irq 0xc io_value_out 0xd:inverted io_value_out 0xe io_value&light_flag inverted others:pin_ctl[10]

bit【7:4】: INT_IRQ pin output function selection

bit【3:0】: IO_VAL pin output function selection

0x24	0x0	R/W	pin_ctl[11:10]	[7:4]	Reserved
				[3]	INT_IRQ GPIO out
				[2]	IO_VAL GPIO out
				[1]	power mode control select 0:by P1_5 1:by CPU control register
				[0]	ADC1 sample enable for VCO tuning 0:enable

bit【3】: 1 outputs high and 0 outputs low when the INT_IRQ pin is set to GPIO output function

bit【2】: IO_VAL pin set to GPIO output function, 1 output high, 0 output low

bit【1】: Regular power consumption and low-power mode selection, use the external pin to select the gear mode or CPU register control mode

bit【0】: Enable ADC1 to be used as configuration input for VCO frequency trimming

0x25	0x20	R/W	ls_delay	[7]	Reserved
				[6:0]	light sensor triger signal delay

bit【6：0】：Set the delay time of photosensitive trigger signal

6.12. Schematic diagram

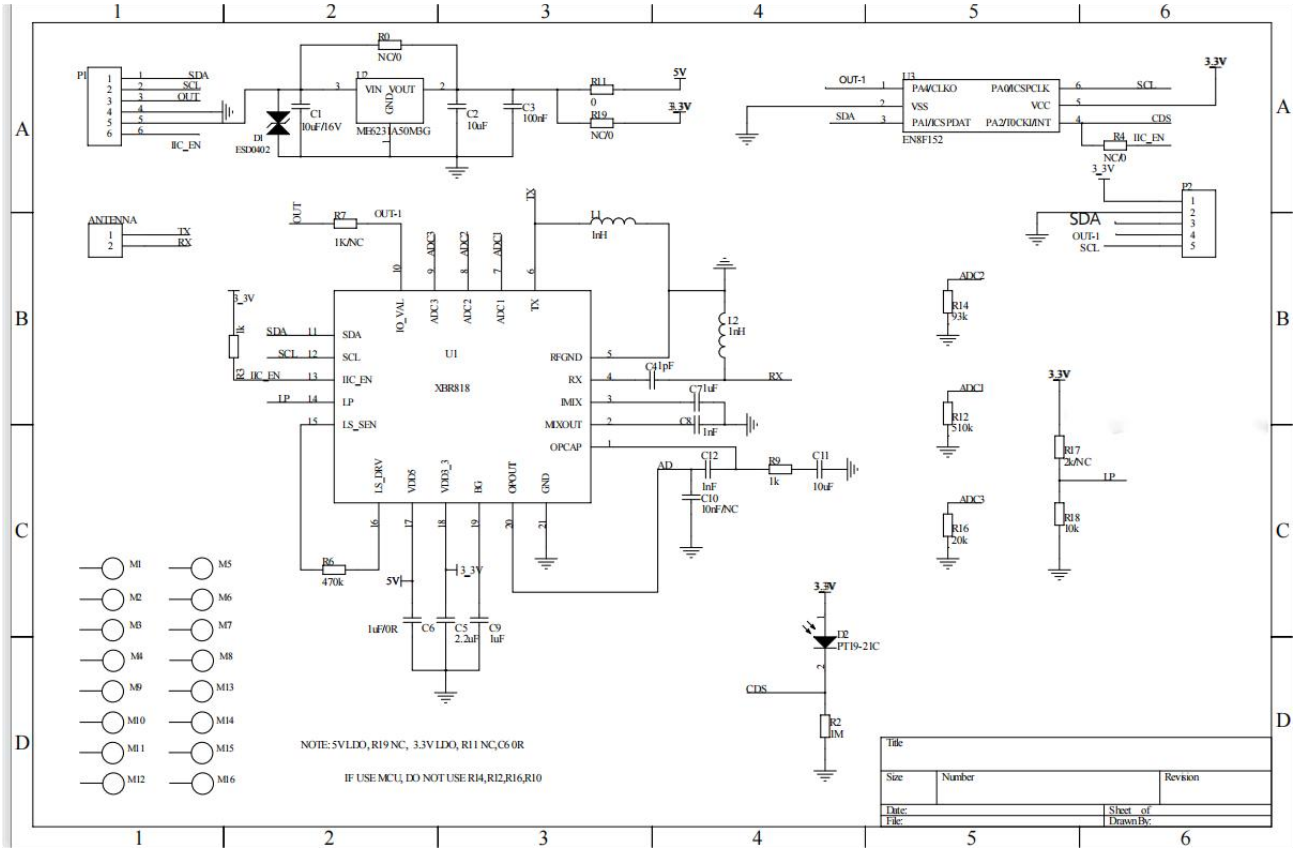


Figure 5 Rd-04 schematic diagram

7. Radar installation and installation instructions

7.1. Radar installation mode

■ Top-hanging installation mode

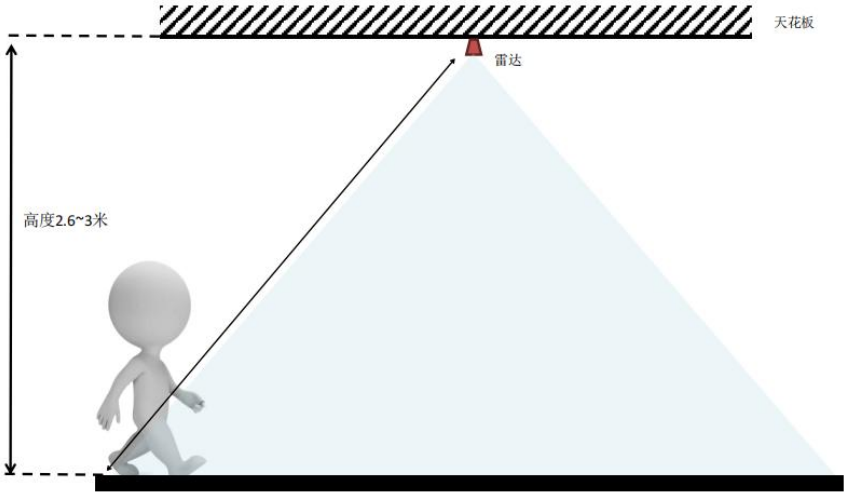
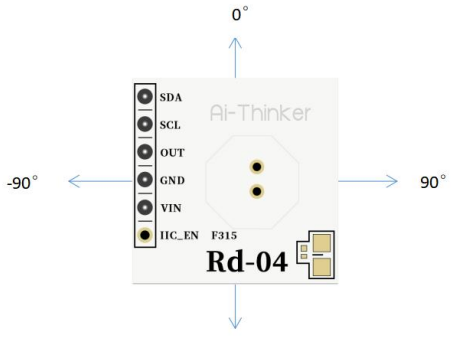


Figure6 Schematic diagram of the top-hanging installation



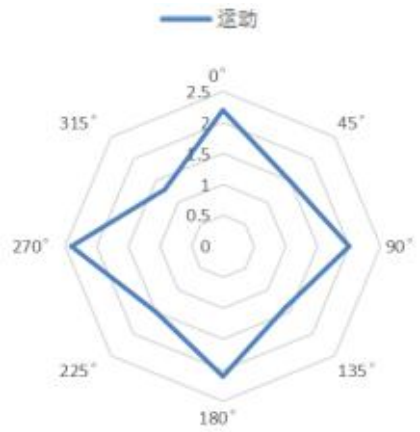
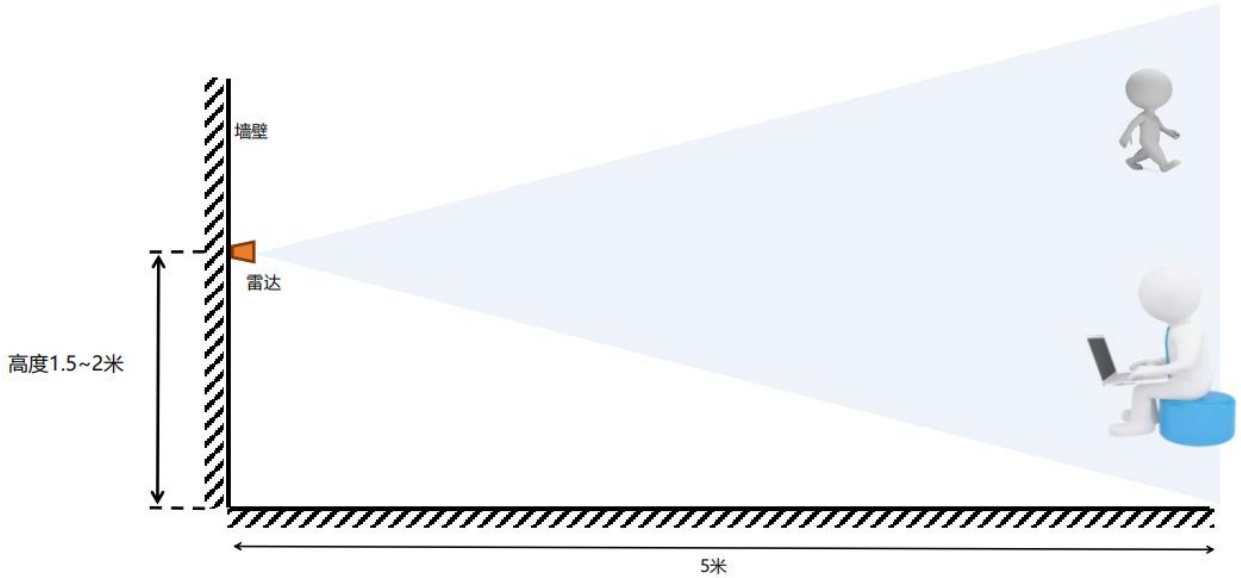


Figure7 Schematic diagram of the detection range of the top-hanging installation

■ Wall-hanging installation mode



Fugure8 Schematic diagram of the wall-hanging installation

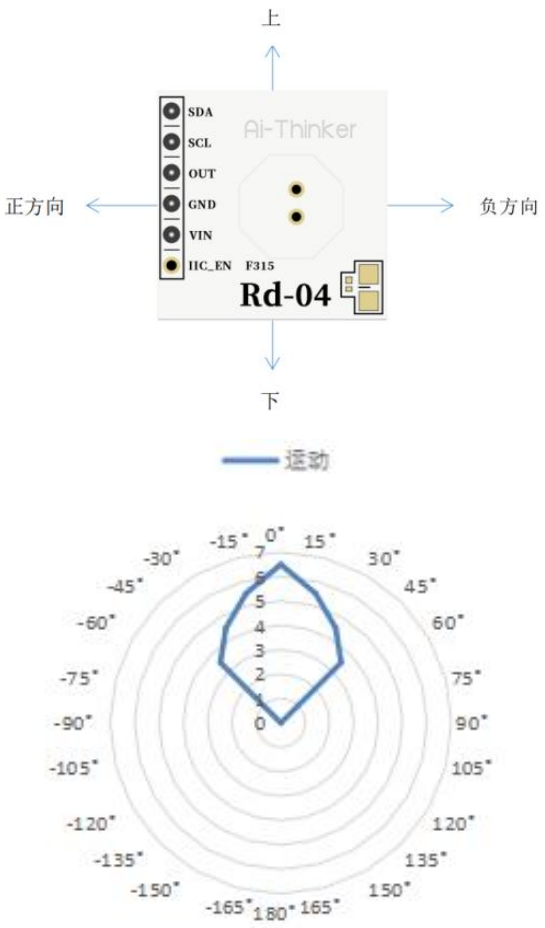


Figure 9 Schematic diagram of the detection range for the wall-hanging installation

7.2. Radar installation instructions

7.2.1. Precautions for radar installation

- In the installation position on the motherboard, the following ways are recommended:：

✓ Try to ensure that the radar antenna is facing the area to be detected, and the antenna is open without shielding;

✓ To ensure that the radar installation position is firm and stable, the shaking of the radar itself will affect the detection effect;

✓ In the case of walls or obstacles reflecting microwave, the perceived distance and perceived Angle will gain;

✓ In the open environment, the perception distance and Angle will be attenuated; because the microwave antenna can be changed detection by a small change, please protect the antenna, the surface without metal objects (such as solder wire), to avoid affecting the perception distance;

✓ The radar module maintains an independent use space, and the surrounding space maintains a free space interval of more than 2mm;

✓ About 15s initialized noise analysis time after power-on, during which it is abnormal perception work;

✓ During production line testing and aging operation, if a large number of radar modules are stacked to a block, there may be self-excitation phenomenon. Please ensure that a safe distance of more than 50cm is maintained between the powered radar modules.

- In order to meet the performance of on-board antenna, metal parts are prohibited around the antenna, away from high-frequency devices.

7.2.2. Radar installation environment requirements

The product needs to be installed in the suitable environment, if used in the following environment, the test effect will be affected:

- There are non-human objects with continuous movement in the induction area, such as animals, curtains that keep swinging, and large green plants facing the air outlet.
- There is a large area of strong reflector in the induction area, which can cause interference to the radar antenna.

- When installing the hanging wall, it is necessary to consider the external interference factors such as the air conditioning and electric fan on the top of the room.

7.2.3. Note for device application and installation of built-in radar module

- ✓ Equipped with radar module components, the installation position should be far away from the ventilation pipe, fire pipe, drainage pipe, mechanical vibration or large metal equipment and other strong vibration objects;
- ✓ Live operation is strictly prohibited, so as to avoid action error, connection error, burn out the circuit or electric shock;
- ✓ Avoid installation in the sun and rain, to prevent damage and affect the service life;
- ✓ Devices must be installed away from the electromagnetic field to avoid electromagnetic interference and misoperation; they should also be installed away from objects fixed rotating or swinging (such as electric fan, swaying leaves, drying clothes in the wind, etc.) to avoid misoperation;
- ✓ When the devices of several built-in radar modules are fixed, the spacing between each device shall be ≥ 0.5m;
- ✓ The antenna surface of the radar microwave module is recommended to be 3~5mm away from the product shell, otherwise it will affect the perception distance;

Figure10 Distance between the antenna surface and the product shell

- ✓ After the built-in radar module, it is recommended to place it horizontally or vertically. Within the effective perception range, try to avoid installing two or more built-in radar modules face to face;
- ✓ If the device using the built-in radar module (such as lamps) is always working (always bright) and cannot be turned on and off according to the moving target detection, the radar module may be disturbed by moderate frequency, causing the module to be judged to have a moving target moving within the perception range. At this time, the power supply should be turned off to check whether the power supply state of the power board is normal and whether the module space distance changes;

- ✓ If the above problems cannot be solved, please power off and observe the situation around the installation position, and eliminate the influence of environmental interference factors; after starting the power supply, replace the drive power panel or radar module.

8. Main parameter

Table5 Description of main parameters

Model	Rd-04
Package	DIP
Size	15.0*15.0mm
Antenna	On-board antenna
Spectrum range	10.275-10.775GHz
Working temperature	-40℃ ~ 85℃
Storage environment	-40℃ ~ 125℃, < 90%RH
Power supply range	3.0V ~ 3.6V，current ≥100mA
Support interface	IIC
IO	2

8.1. Electrostatic requirements

Rd-04 is a static sensitive device and requires special precautions when handling it.

Figure 11 ESD Anti-static diagram

8.2. Radar sensing distance

Install method	Min. value	Typ. value	Max. value	Unit
Wall-mounted way (radial)	-	6.5	-	m

Wall-hanging method (3m high), circular projection radius	-	2.5	-	m

Table 6 Radar sensing distance

8.3. Electrical character

Table 7 Eelectrical character

Parater		Condition	Min. value	Typ. value	Max. value	Unit
Supply Voltage		VDD	3.0	3.3	3.6	V
I/O	VIL	-	-	-	0.3*VDDIO	V
	VIH	-	0.7*VDDIO	-	-	V
	VOL	-	-	0.1*VDDIO	-	V
	VOH	-	-	0.9*VDDIO	-	V
	IMAX	-	-	-	15	mA

8.4. Power consumption

The following power consumption data are based on the 3.3V power supply and the ambient temperature of 25°C.

Table 8 Power consumption table

Mode	Min. value	Average value	Max. value	Unit
Regular power supply mode	-	16	-	mA
Pulse power supply mode	-	110	-	μA

9. Contact us

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