



# Ai-BV01-32S Specification

Version V1.2.1

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## Contents

1. Product Overview .....	4
1.1. Features .....	5
2. Main Parameters .....	5
2.1. Static Electricity Requirements .....	6
2.2. Electrical Characteristics .....	6
2.3. BR/EDR RF Performance .....	6
2.4. BLE RF Performance .....	7
2.5. Power Consumption .....	8
3. Appearance and Dimensions .....	9
4. Pin Definition .....	10
5. Schematic Diagram .....	14
6. Antenna Parameters .....	15
6.1. Antenna Test Prototype .....	15
6.2. Antenna S-Parameters .....	15
6.3. Antenna Gain and Efficiency .....	16
6.4. Antenna Pattern Diagram .....	16
7. Design Guide .....	17
7.1. Application Circuit .....	17
7.2. Recommended PCB Footprint Dimensions .....	18
7.3. Antenna Layout Requirements .....	18
7.4. Power Supply .....	19
7.5. GPIO .....	19
8. Storage Conditions .....	20
9. Reflow Soldering Profile .....	20
10. Packaging Information .....	21
11. Contact Information .....	21
Disclaimer and Copyright Notice .....	22
Notice .....	22
Statement .....	23

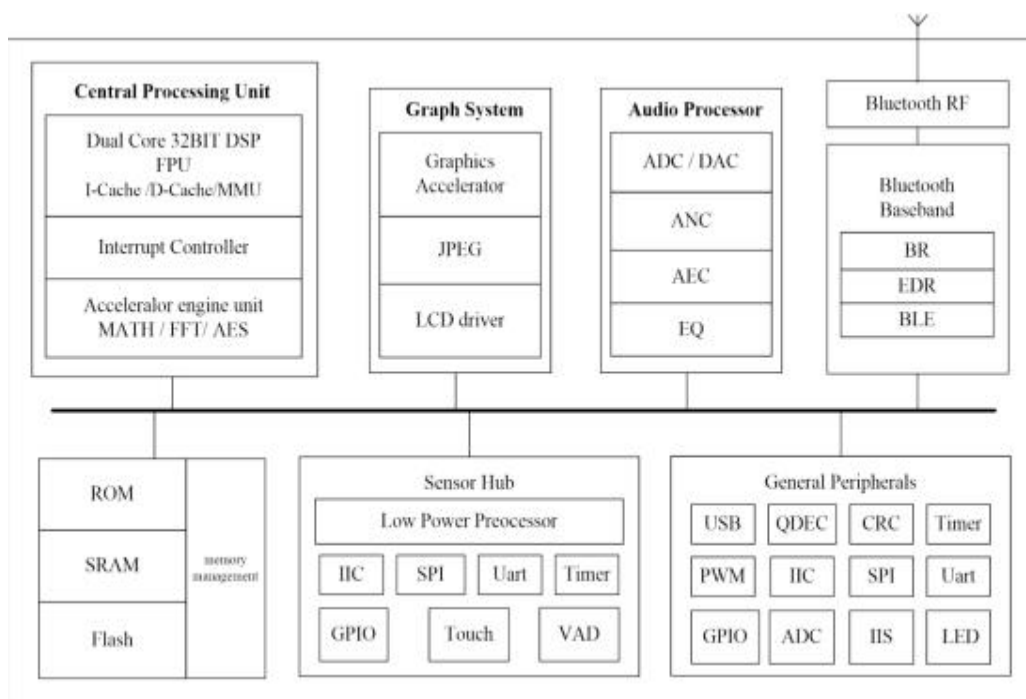
# 1. Product Overview

Ai-BV01-32S is an artificial intelligence AIoT voice module developed by Shenzhen Ai-Thinker Technology Co., Ltd. This module supports dual-mode Bluetooth V5.4+BR+EDR+BLE specification, featuring high performance, high reliability, and strong versatility. In AI speech algorithms, it achieves enhanced noise reduction performance, highly reliable wake-up recognition rate, and high-definition call quality. It also supports a richer set of offline speech control commands, faster response recognition time, and hybrid offline + online recognition capability.

The Ai-BV01-32S module is equipped with the VB7014F chip as its core processor, which utilizes a dual-core 32-bit audio processor, integrates a dedicated audio DSP core, and supports acceleration for artificial intelligence neural network algorithms.

The VB7014F chip integrates dual-mode Bluetooth and complies with Bluetooth V5.4+BR+EDR+BLE specification. It supports BLE connectivity to smartphone Bluetooth apps or mini programs, BR/EDR connection to smartphones for Bluetooth audio playback, and hardware floating-point arithmetic, with built-in 4 MB Flash.

The Ai-BV01-32S module features a rich set of peripheral interfaces, including USB 2.0, SPI, UART, I2C, PWM, DAC, ADC, and GPIO. It can be widely applied in various fields such as audio-video multimedia, the Internet of Things (IoT), mobile devices, wearable electronics, and smart home systems.



**Figure 1 Main Chip Architecture Diagram**

## 1.1. Features

- Adopts SMD-40 package
- Supports 2.4 GHz operating frequency band
- Supports Bluetooth V5.4+BR+EDR+BLE
- Supports automatic speech recognition (ASR) algorithm
- Supports speech noise reduction algorithm
- Supports echo cancellation algorithm
- Integrates built-in 4 MB Flash
- Supports reliable recognition within 5 meters
- Supports background noise suppression
- Supports universal AT commands for quick start
- Supports secondary development and integrates Windows and Linux development environments.

## 2. Main Parameters

**Table 1 Main Parameter Specifications**

<b>Model</b>	Ai-BV01-32S
<b>Package</b>	SMD-40
<b>Dimensions</b>	25.5*18.0*3.1 mm
<b>Antenna Type</b>	Onboard antenna/IPEX connector
<b>Frequency Range</b>	2400–2483.5 MHz
<b>Operating Temperature</b>	-40–85 °C
<b>Storage Conditions</b>	-40–125 °C , < 90% RH
<b>Power Supply Range</b>	VDD: 2.5–4.5 V, supply current $\geq 200$ mA; DACLP/5V: 2.5–6 V, supply current $\geq 1$ A
<b>Supported Interfaces</b>	USB2.0, SPI, UART, I2C, PWM, ADC and GPIO
<b>Available I/Os</b>	Default 26
<b>UART Baud Rate</b>	Default 2000000bps
<b>Flash</b>	Default 4MByte

## 2.1. Static Electricity Requirements

Ai-BV01-32S is an ESD-sensitive device and requires special precautions during handling.



Figure 2 ESD Protection Symbol

## 2.2. Electrical Characteristics

Table 2 Electrical Characteristics

Parameter	Condition	Min	Typ	Max	Unit	
Power Supply	VDD	2.5	3.3	4.5	V	
Power Supply	DACL P/5V	2.5	5	6	V	
I/O	VIL	-	-0.3	-	0.9	V
	VIH	-	2.1	-	3.6	V
	VOL	-	-	-	0.3	V
	VOH	-	2.7	-	-	V
	IMAX	-	-	8	46	mA

## 2.3. BR/EDR RF Performance

Table 3 BR/EDR RF Performance

Description	Typ			Unit
Frequency Range	2400–2483.5			MHz
Output Power				
Mode	Min	Typ	Max	Unit
DH1	-	6	-	dBm
DH3	-	6	-	dBm
DH5	-	6	-	dBm
Receiver Sensitivity				
Mode	Min	Typ	Max	Unit
BR(1-DH1)	-	-92	-	dBm
BR(1-DH3)	-	-92	-	dBm

BR(1-DH5)	-	-92	-	dBm
EDR(2-DH1)	-	-94	-	dBm
EDR(2-DH3)	-	-94	-	dBm
EDR(2-DH5)	-	-94	-	dBm
EDR(3-DH1)	-	-88	-	dBm
EDR(3-DH3)	-	-88	-	dBm
EDR(3-DH5)	-	-88	-	dBm

## 2.4. BLE RF Performance

**Table 4 BLE RF Performance**

Description	Typ			Unit
Frequency Range	2400–2483.5			MHz
<b>Output Power</b>				
Data Rate Mode	Min	Typ	Max	Unit
1 Mbps	-	6	-	dBm
2 Mbps	-	6	-	dBm
<b>Receiver Sensitivity</b>				
Data Rate Mode	Min	Typ	Max	Unit
1 Mbps Sensitivity @30.8% PER	-	-97	-	dBm
2 Mbps Sensitivity@30.8% PER	-	-94	-	dBm

## 2.5. Power Consumption

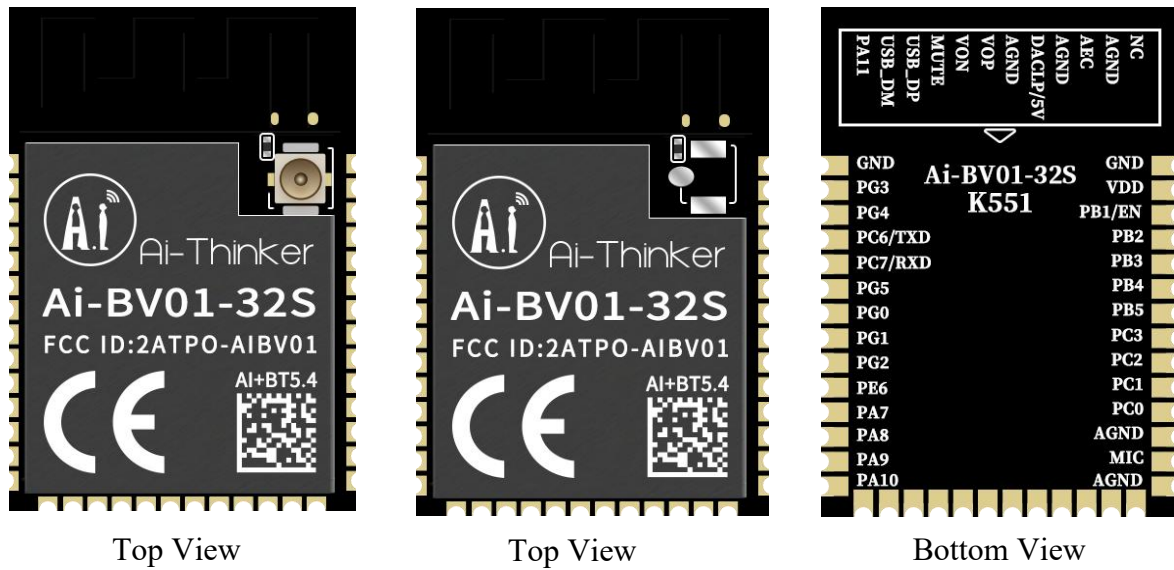
The following power consumption data is measured based on a 3.3 V power supply and an ambient temperature of 25 °C.

- The POUT power for all transmit modes is measured at the antenna interface.

**Table 5 Power Consumption**

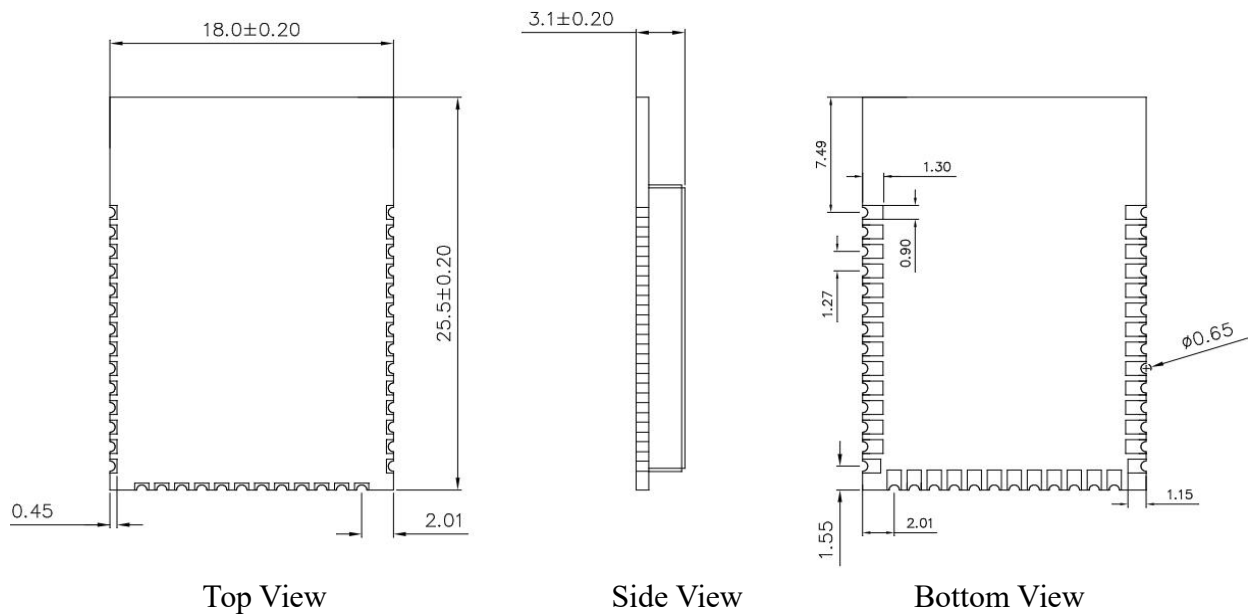
Mode	Min	Avg	Max	Unit
TX DH1, Pn9, Pout = 6 dBm	-	20	-	mA
TX DH3, Pn9, Pout = 6 dBm	-	33	-	mA
TX DH5, Pn9, Pout = 6 dBm	-	37	-	mA
TX PHY=1 M, PRBS9, Pout = 6 dBm	-	12	-	mA
TX PHY=2 M, PRBS9, Pout = 6 dBm	-	11	-	mA
BR/EDR RX DH1	-	5	-	mA
BR/EDR RX DH3	-	5	-	mA
BR/EDR RX DH5	-	5	-	mA
BLE RX PHY=1 M	-	26	-	
BLE RX PHY=1 M	-	26	-	

### 3. Appearance and Dimensions



**Figure 3 Appearance Diagram**

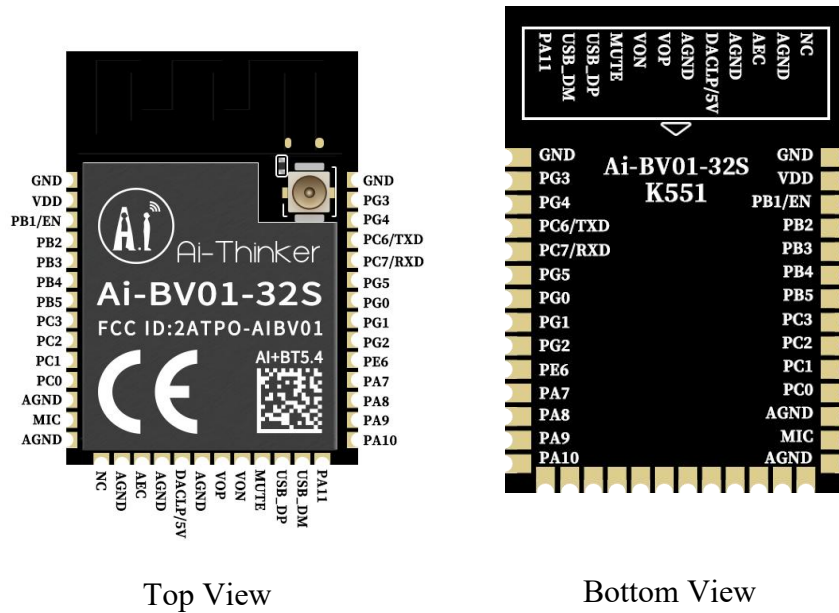
(Rendering for reference only; actual product may vary)



**Figure 4 Dimension Diagram (Unit: mm)**

## 4. Pin Definition

The Ai-BV01-32S module exposes a total of 40 pins, as shown in the pin diagram. The pin function definition table provides the detailed interface specifications.



**Figure 5 Pin Diagram**

**Table 6 Pin Function Definition**

No.	Name	Function Description
1	GND	Ground
2	VDD	2.5–4.5 V power supply; external power supply output current is recommended to be above 200 mA
3	PB1/EN	Hold down 0 to reset ADC6: ADC Input Channel 6
4	PB2	ADC7: ADC Input Channel 7 UART3TXA: UART3 Data Output (A) SPI4CLKA: SPI4 Clock (A) CAP5: Timer 5 Capture
5	PB3	UART3RXA: UART3 Data Input (A) SPI4DOA: SPI4 Data Out (A)

6	PB4	CLKOUT0: Clock Out0 IIC1_SCL_A: IIC1 SCL (A) UART3TXB: UART3 Data Output (B) SPI4DIA: SPI4 Data In (A) TMR2: Timer 2 Clock Input
7	PB5	IIC1_SDA_A: IIC1 SDA (A) ADC8: ADC Input Channel 8 UART3RXB: UART3 Data Input (B)
8	PC3	TMR3: Timer 3 Clock Input
9	PC2	TMR1: Timer 1 Clock Input
10	PC1	TMR5: Timer 5 Clock Input PWMCH1L: Motor PWM Channel 1 (L)
11	PC0	PWMCH1H: Motor PWM Channel 1 (H)
12	AGND	AGND; it is recommended to connect to the microphone input negative terminal
13	MIC	Microphone input positive terminal
14	AGND	AGND
15	NC	NC
16	AGND	AGND
17	AEC	Audio echo cancellation input, connected to the chip's REC_P
18	AGND	AGND
19	DACLP/5V	Left channel audio output positive/5 V input for the power amplifier. When using a DAC to output to an external power amplifier, the function is DACLR; when using the module's internal power amplifier, the function is power amplifier power input. Accepts 2.5–6 V input, with 5 V recommended. Recommended current is 1 A or higher.
20	AGND	AGND
21	VOP	Amplifier output P
22	VON	Amplifier output N
23	MUTE	Speaker mute control pin. This pin is internally connected to the EN control pin of the onboard amplifier within the module. When using an

		external amplifier for the module, this pin can be connected to the EN control pin of the external amplifier
24	USB_DP	PA15 USB Positive Data SPI2CLKB: SPI2 Clock (B) IIC0_SCL_A: IIC0 SCL (A) ADC10: ADC Input Channel 10 UART1TXB: UART1 Data Output (B)
25	USB_DM	PC8: SPI2DIB: SPI2 Data In (B) USB Negative Data SPI2DOB: SPI2 Data Out (B) IIC0_SDA_A: IIC0 SDA (A) ADC11: ADC Input Channel 11 UART1RXB: UART1 Data Input (B)
26	PA11	GPIO
27	PA10	GPIO
28	PA9	PWMCH0H: Motor PWM Channel 0 (H)
29	PA8	ADC3: ADC Input Channel 3 UART2RXB: UART2 Data Input (B)
30	PA7	UART2TXB: UART2 Data Output (B) TMR0: Timer 0 Clock Input
31	PE6	PE5/PE6 SDPG: SD card power gate
32	PG2	SD0_CLKB: SD0 Clock (B) PWMCH2L: Motor PWM Channel 2 (L)
33	PG1	SD0_CMDB: SD0 CMD (B) ADC13: ADC Input Channel 13 PWMCH2H: Motor PWM Channel 2 (H)
34	PG0	SD0_DATB: SD0 Data (B) ADC12: ADC Input Channel 12

35	PC5	IIC0_SDA_B: IIC0 SDA (B) ADC5: ADC Input Channel 5 UART2RXA: UART2 Data Input (A)
36	PC7/RXD	GPIO (High Voltage Resistant) RXD
37	PC6/TXD	GPIO (High Voltage Resistant) TXD
38	PG4	PWMCH3L: Motor PWM Channel 3 (L)
39	PG3	PWMCH3H: Motor PWM Channel 3 (H)
40	GND	GND

Notes:

1. PC6 and PC7 are high-voltage-tolerant I/O pins. They can be connected to a 5 V level, with a maximum withstand voltage of 5 V.
2. For VOP and VON, it is recommended to use 4Ω3W and 8Ω2W speakers.
3. An electret microphone must be used.
4. DACLP/5V is the default power supply input pin for the amplifier. To use DACLR to drive an external amplifier, please contact Ai-Thinker.



## 6. Antenna Parameters

### 6.1. Antenna Test Prototype

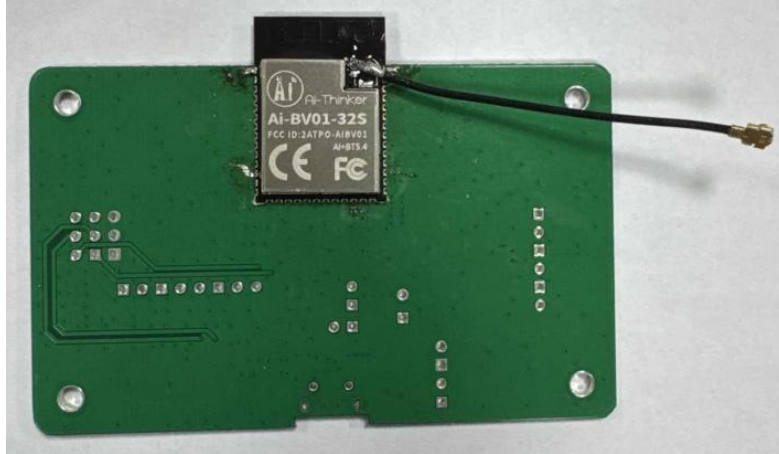


Figure 7 Antenna Test Prototype

### 6.2. Antenna S-Parameters

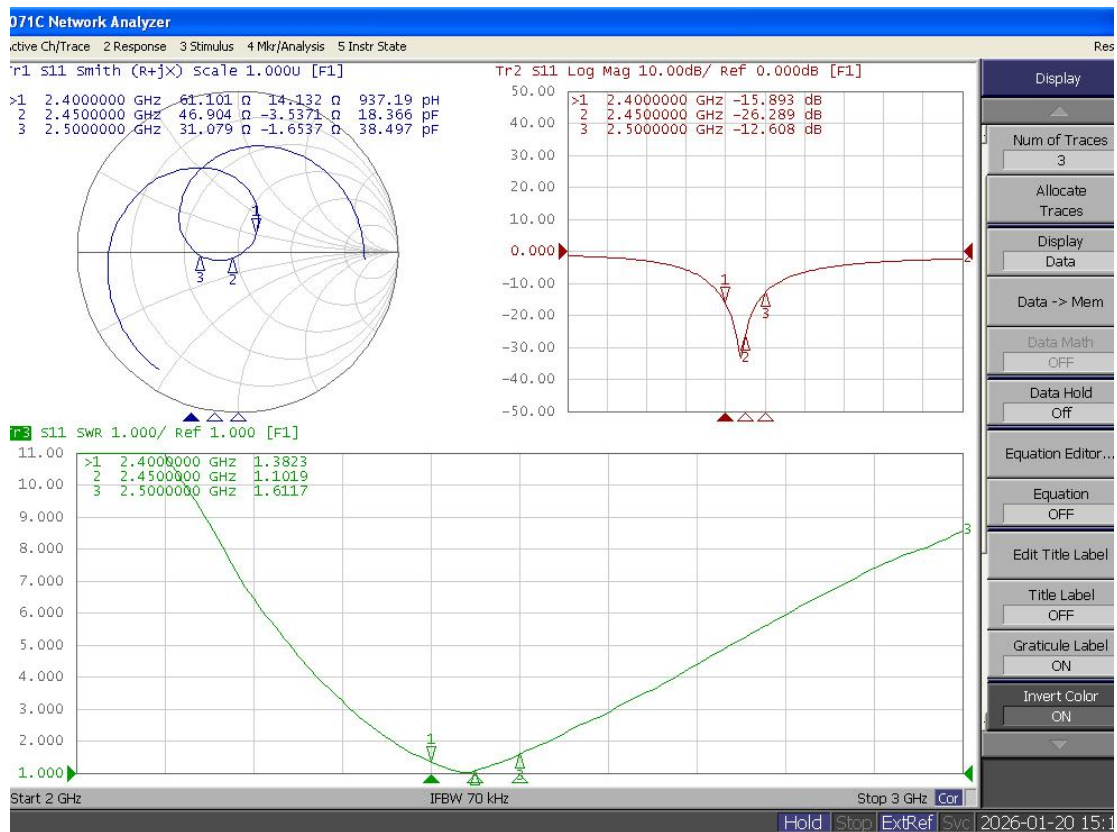


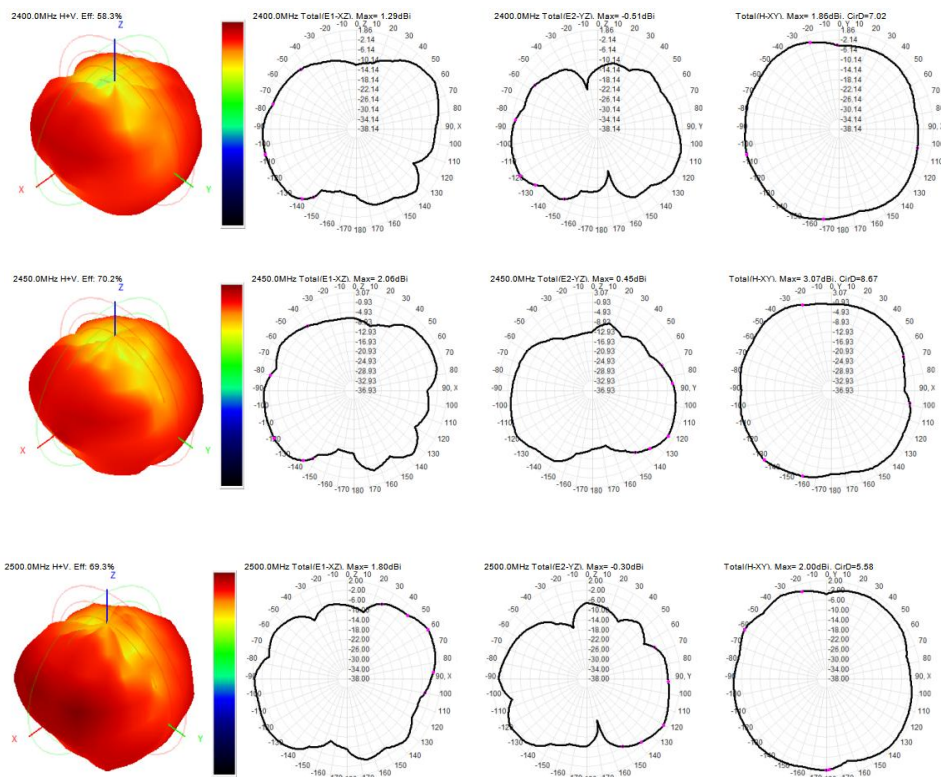
Figure 8 Antenna S-Parameters

### 6.3. Antenna Gain and Efficiency

**Table 7 Antenna Gain and Efficiency**

Frequency ID	1	2	3	4	5	6	7	8	9	10	11
Frequency (MHz)	2400.0	2410.0	2420.0	2430.0	2440.0	2450.0	2460.0	2470.0	2480.0	2490.0	2500.0
Gain (dBi)	2.17	2.34	2.56	2.30	2.74	3.07	2.30	2.29	2.88	2.54	2.30
Efficiency (%)	58.31	60.47	62.75	63.82	69.45	70.16	68.90	68.68	70.40	67.81	69.31

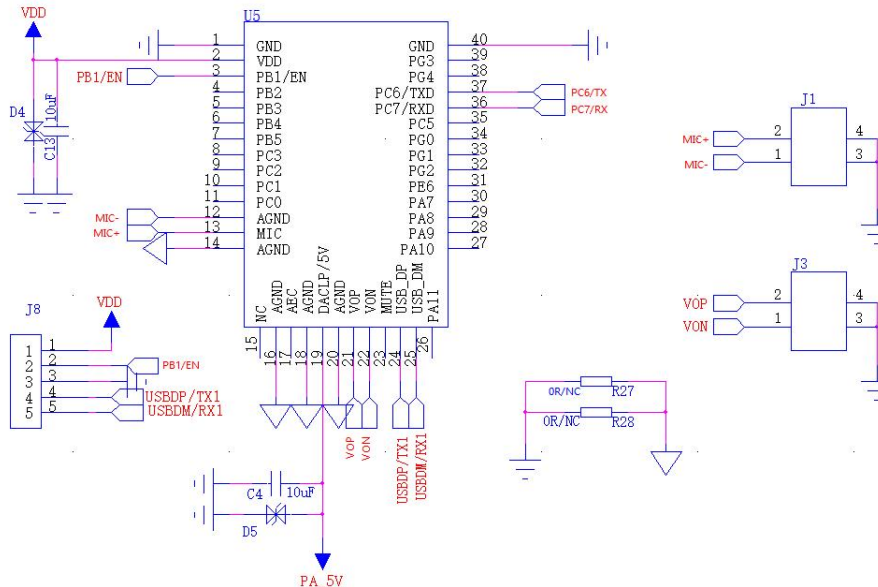
### 6.4. Antenna Pattern Diagram



**Figure 9 Antenna Pattern**

## 7. Design Guide

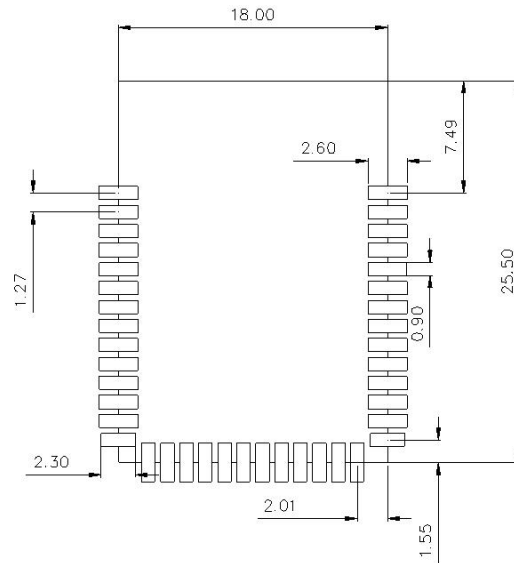
### 7.1. Application Circuit



**Figure 10 Application Circuit**

- USB\_DM and USB\_DP are the module's default programming pins.
- PC6 and PC7 are the module's default primary communication UART and high-voltage-tolerant I/O ports, which can be connected to a 5 V level.
- MIC+ connects to the microphone positive terminal, and MIC- connects to the microphone negative terminal.
- VOP and VON connect to speakers. Speakers with 4Ω3W or 8Ω2W are recommended.
- VDD: Supply voltage range is 2.5–4.5 V; the external power supply output current is recommended to be above 200 mA.
- DACLP/5V: Supply voltage range is 2.5–6 V; the external power supply output current is recommended to be above 1 A.

## 7.2. Recommended PCB Footprint Dimensions



**Figure 11 Recommended PCB Footprint Dimensions (Unit: mm)**

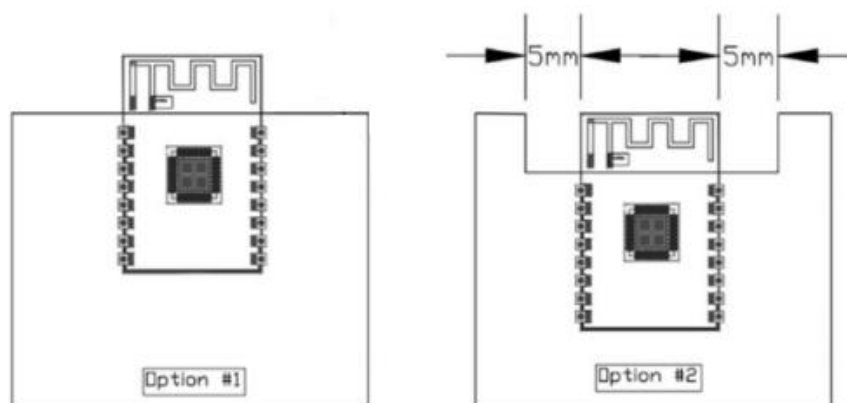
## 7.3. Antenna Layout Requirements

- For the installation position on the mainboard, the following 2 options are recommended.

Option 1: Place the module at the mainboard edge, with the antenna area extending beyond it.

Option 2: Place the module at the mainboard edge, with a clearance cutout at the antenna position.

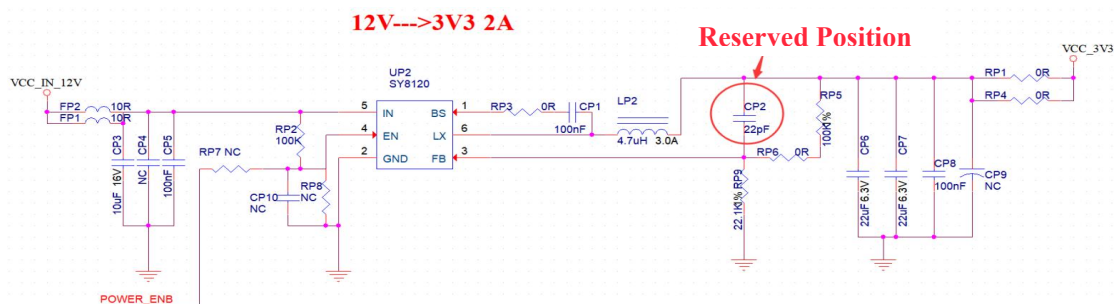
- To ensure optimal performance of the onboard antenna, metal objects must not be placed near the antenna, and the antenna should be kept away from high-frequency devices.



**Figure 12 Antenna Layout Diagram**

## 7.4. Power Supply

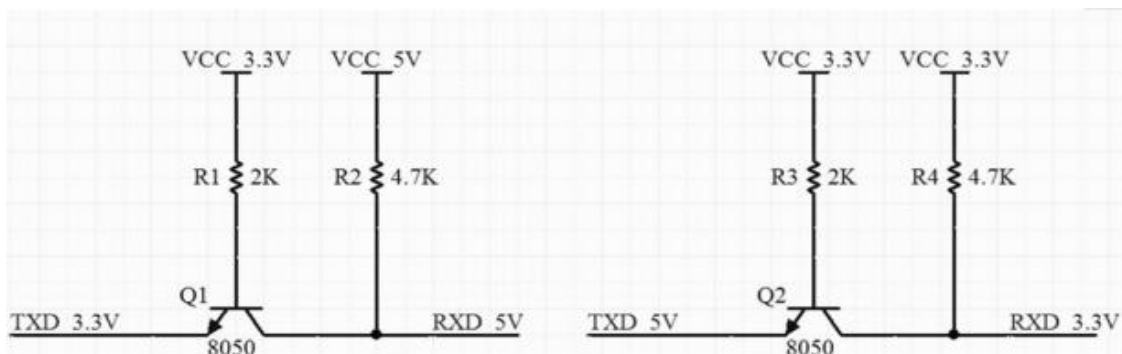
- VDD is recommended as 3.3 V, with a peak current above 200 mA.
- DACLP/5V is recommended as 5 V, with a peak current above 1 A
- An LDO is recommended for power supply; if using DC-DC, the ripple should be controlled within 30mV.
- For the DC-DC power supply circuit, it is recommended to reserve space for dynamic response capacitors to optimize output ripple under large load transients.
- It is recommended to add ESD protection devices at the power interface.



**Figure 13 DC-DC Buck Circuit**

## 7.5. GPIO

- Some I/O pins are exposed on the module periphery. To use these I/O pins, it is recommended to connect a 10-100Ω resistor in series with each I/O pin. This helps suppress overshoot, stabilize signal levels, and benefits both EMI and ESD protection.
- The pull-up or pull-down configuration for specific I/O pins must follow the guidelines in the specification, as it affects the module’s boot configuration.
- The module’s I/O pins operate at 3.3 V. If the I/O voltage level of the main controller and the module do not match, a level-shifting circuit must be added.
- If an I/O pin is directly connected to a peripheral interface or pin headers, it is recommended to reserve space for an ESD protection device near the connector on the I/O trace.



**Figure 14 Level-shifting Circuit**

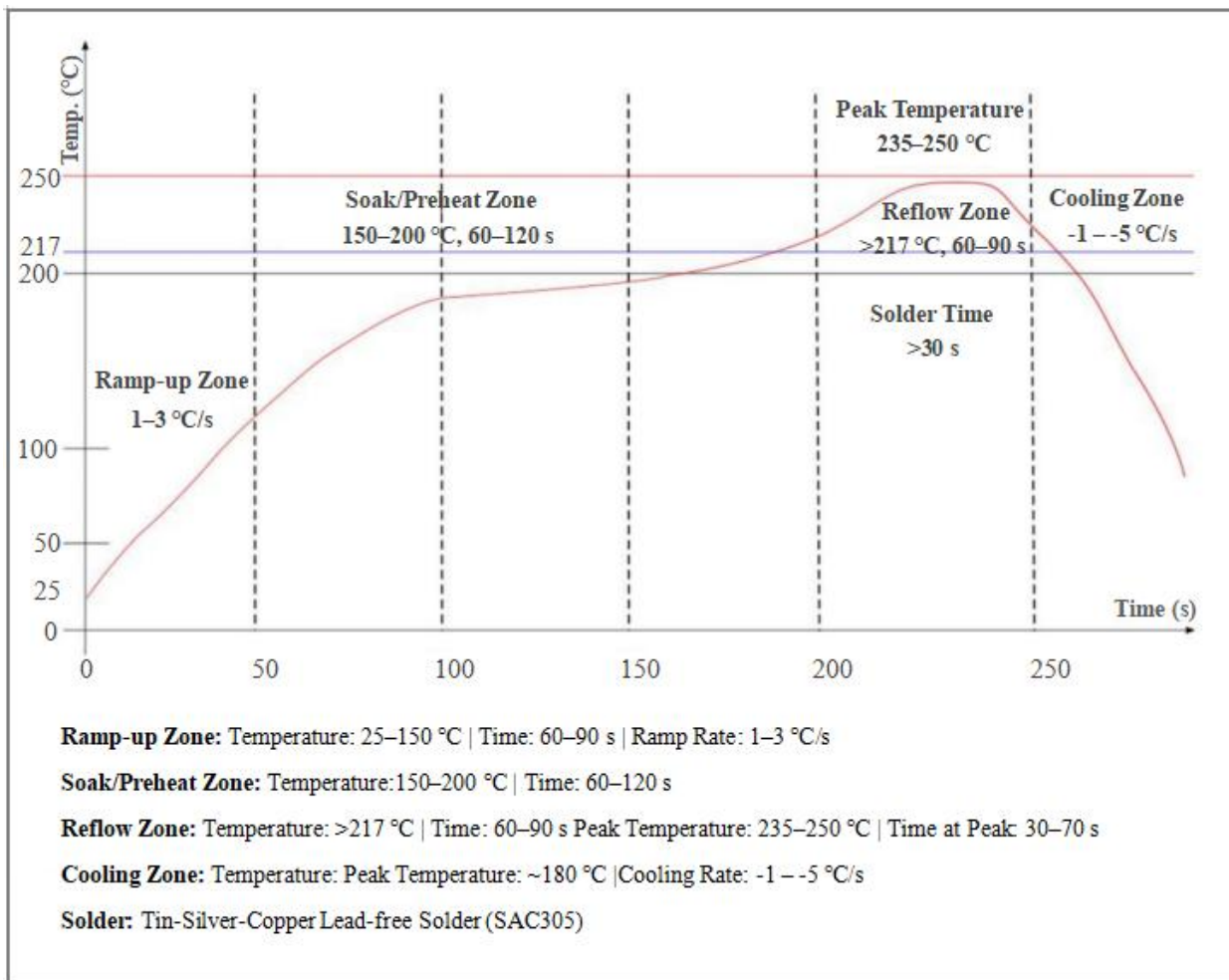
## 8. Storage Conditions

Products sealed in moisture barrier bags should be stored in a non-condensing atmosphere at <math><40\text{ }^\circ\text{C}</math> and <math><90\% \text{ RH}</math>.

The moisture sensitivity level (MSL) of the module is level 3.

The module must be used within 168 hours after vacuum bag removal under conditions of

## 9. Reflow Soldering Profile



**Figure 15 Reflow Soldering Profile**

## 10. Packaging Information

The Ai-BV01-32S module is packaged in tape and reel, 800 pcs/reel, as shown below.



Figure 16 Tape and Reel Packaging Diagram

## 11. Contact Information

[Official Website](#)

[Official Forum](#)

[Development DOCS](#)

[LinkedIn](#)

[Tmall Store](#)

[Taobao Store](#)

[Alibaba Store](#)

[Technical Support: support@aithinker.com](mailto:support@aithinker.com)

[Domestic Business Cooperation: sales@aithinker.com](mailto:sales@aithinker.com)

[Overseas Business Cooperation: overseas@aithinker.com](mailto:overseas@aithinker.com)

Company Address: Room 403–405, 408–410, Building C, Huafeng Smart Innovation Port, Gushu, Xixiang, Bao'an District, Shenzhen, Guangdong, China

Contact Hotline: 0755-29162996



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