LCD MODULE

SPECIFICATION

Model:	UE035QV-RB30-A079A
Version:	V1.0
Date:	20220819

Customer Confirmation 客户确认

Approved by	Notes

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VIEWE Confirmation 优奕确认

Prepared by	Reviewed by	Approved by

REVISION HISTORY

Revision 版本号	Date 日期	Contents of Revision Change 修改内容	Remark 备注
V1.0	20220819	Preliminary release	

TABLE of CONTENTS

1. GENERAL INFORMATION

1.1 Features

1) Pixel Arrangement：RGB Vertical Stripe
2) Interface Mode： MCU 8 BIT or 8BIT SPI
3) Driver IC：GC9307N , TOUCH IC:CHSC6540
4) Operation Temperature：-20~70℃
5) Storage Temperature：-30~80℃
6) Backlight Type：White LED
7) Display mode：Normally Black
8) LED life time：30,000 Hours

1.2 Mechanical Specification

Item 项目	Specification 规格	Unit 单位	Remark 备注
Pixel Driving element	IPS TFT	-	-
Screen Size	3.5	Inch	Diagonal
Resolution	240(W)*3(RGB)*320(H)	Dots	-
Interface	--MCU 8 BIT --8BIT SPI	-	The two interfaces are compatible
Module Power Consumption	0.56	Watt	Typ.
Active Area	51.27(W)*68.36(H)	mm	Typ
Pixel pitch (W*H)	0.213*0.213	mm	Typ
Module Size (W*H*D)	58.91(W)*84 (H)*3.14(D)	mm	Typ
Luminance	350	cd/m^2	Typ.
Viewing Direction	ALL	O'clock	
Display Color	262K	Colors	

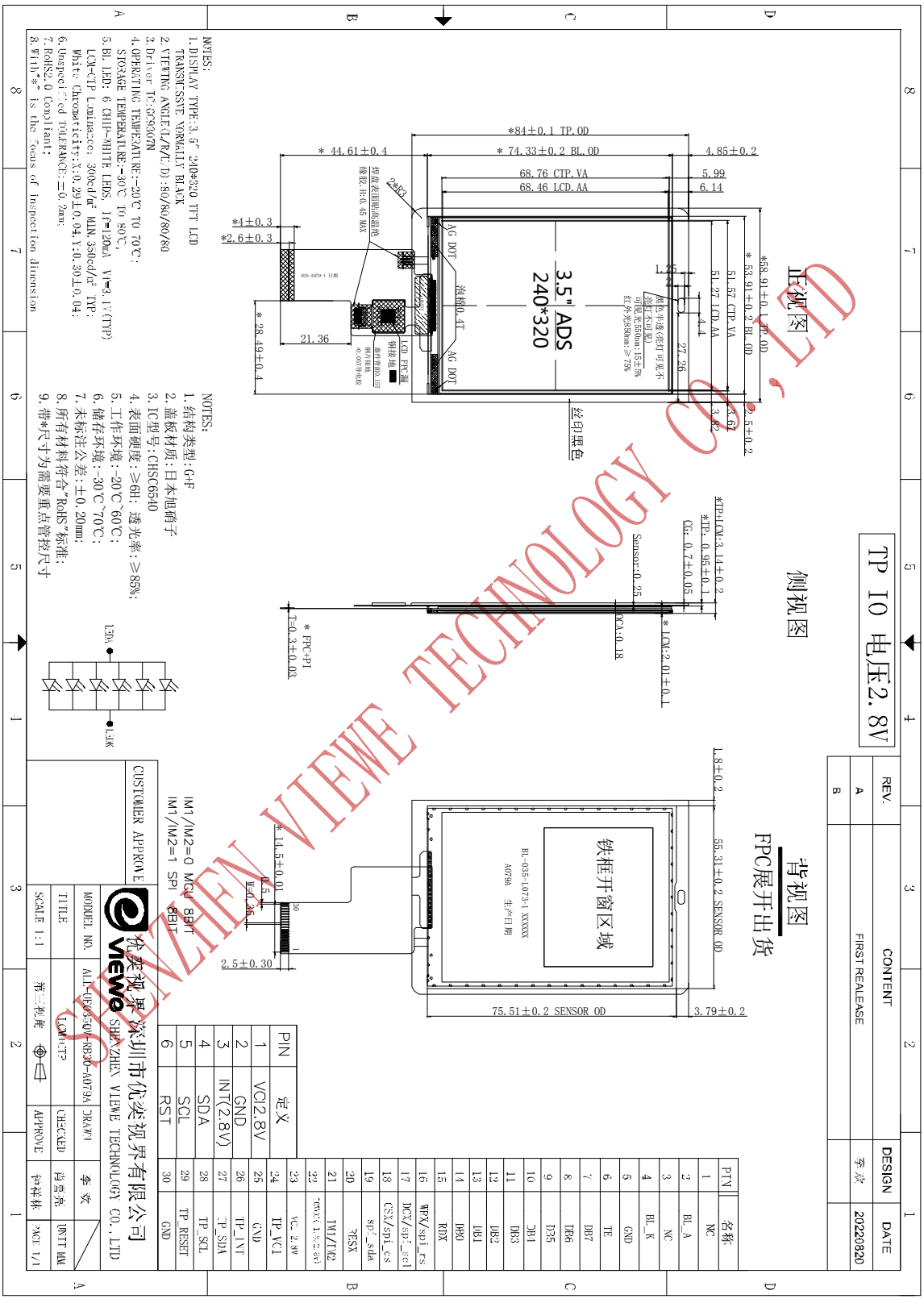
2. ABSOLUTE MAXIMUM RATINGS

Item 项目	Symbol 符号	Min. 最小值	Max. 最大值	Unit 单位	Remark 备注
Power supply1 voltage	IOVCC	-0.3	4.6	V	Note1
Power supply2 voltage	VCI	-0.3	4.6	V	Note1
LED Reverse Voltage	V_R	-	5	V	For each led,Note1

(Ta=+25°C,GND=0V)

Note1:If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

3. MECHANICAL DRAWING



4. I/O CONNECTION & BLOCK DIAGRAM

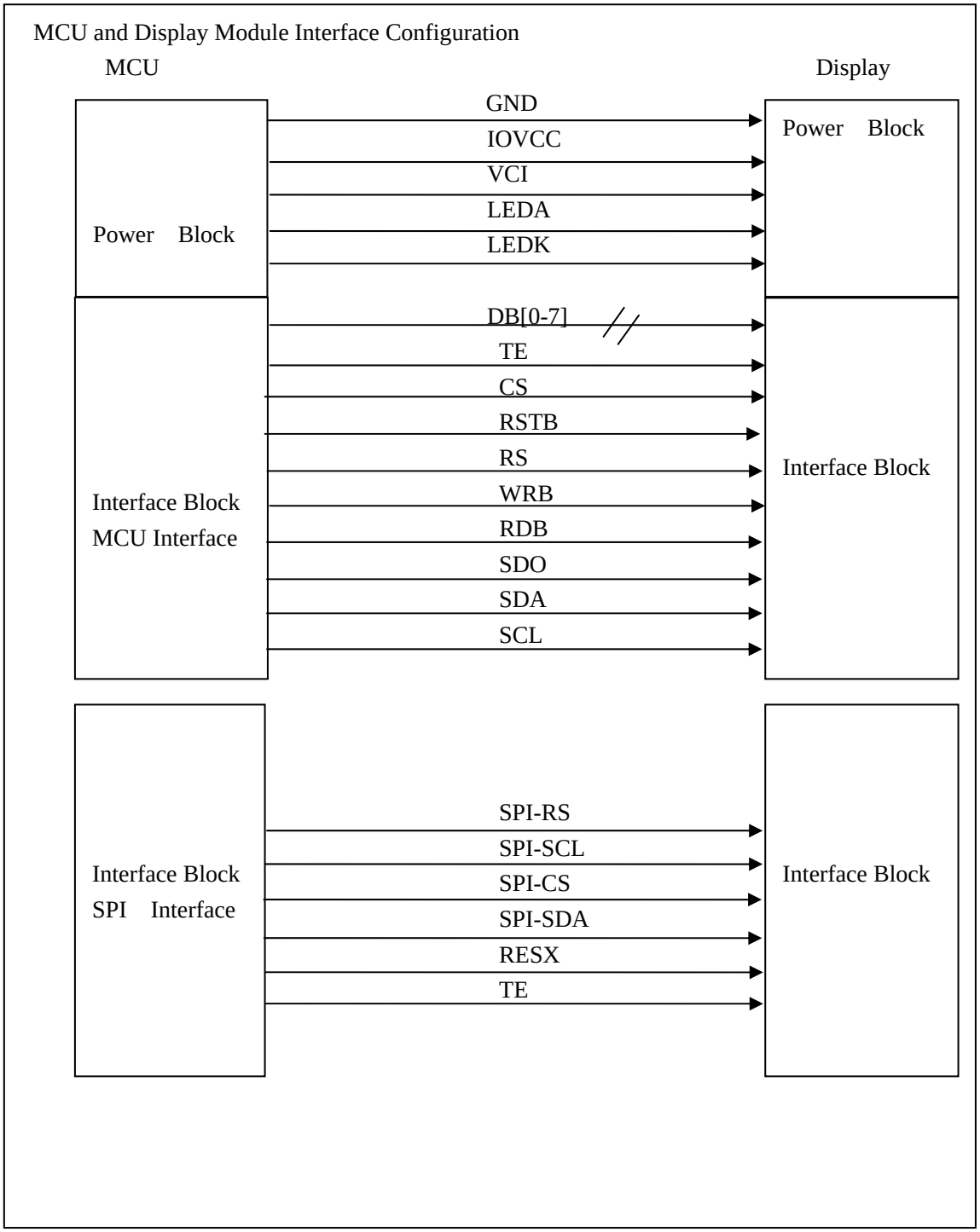
4.1 I/O Connection

Pin No. 序号	Symbol 符号	I/O	Description 描述
1	**NC**		
2	**BL_A**	P	Power supply for backlight anode
3	**NC**		
4	**BL_K**	P	Power supply for backlight cathode
5	**GND**	P	Power Ground
6	**TE**	O	Tearing effect outputsignal. If not used, please let this pin open
7-14	**DB7-DB0**	I	Data input
15	**RDX**	I	Serve as a read data signal
16	**WRX/SPI_RS**	I	Serves as a write data signal
17	**DCX/SPI_SCL**	I	D/C select pin for SPI interface
18	**CSX/SPI_CS**	I	Chip select pin for SPI interface/
19	**SPI_SDA**	I/O	Data select pin for SPI interface
20	**RESX**	I	The signal will reset the LCM, Signal is active low.
21	**IM1/IM2**	I	IM Select
22	**IOVCC(1.8V/2.8V)**	P	Power supply for logic circuits and IO pads
23	**VCI 2.8V**	P	Power supply for analog circuits
24	**TP_VCI**	P	Power supply for analog circuits
25	**GND**	P	
26	**TP_INT**	O	Interrupt signals for TP
27	**TP_SDA**	I/O	I2C data signal for TP
28	**TP_SCL**	I	I2C clock signals for TP
29	**TP_RESET**	I	The signal will reset the TP,Signal is active low
30	**GND**	P	Power Ground

I：Input；O：Output；P：Power

TP PIN .	Symbol	I/O	Description
1	**VCI**	P	Power supply for TP
2	**GND**	P	Power Ground
3	**INT**	O	Interrupt signals for TP
4	**SDA**	I/O	I2C data signal for TP
5	**SCL**	I	I2C clock signals for TP
6	**RST**	I	The signal will reset the TP,Signal is active low

4.2 Block Diagram



5. ELECTRICAL CHARACTERISTICS

5.1 TFT-LCD Panel Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Power Supply1 Voltage	IOVCC	1.65	1.8	3.3	V	-
Power Supply2 Voltage	VCI	2.5	2.8	3.3	V	-
Power Supply1 Current	I_{IOVCC}	-	TBD	-	mA	Note1
Power Supply2 Current	I_{VCI}	-	20	-	mA	Note1
Logic Input High Voltage	V_{IH}	0.7IOVCC	-	IOVCC	V	-
Logic Input Low Voltage	V_{IL}	0	-	0.3IOVCC	V	-
Panel Power Consumption	P_{VDD}	-	0.056	-	Watt	Note1
Module Power Consumption	P_{ALL}	-	0.428	-	Watt	Note1,2

(Ta=+25°C,GND=0V)

Note1:Measurement Conditions (Video Mode): Full Screen Red Pattern,VDD=2.8V,60Hz Refresh.

Note2: P_{ALL}= P_{VDD}+ P_{BL}， About P_{BL} information, inference to 5.2 Back Light Driving Section.

5.2 Back Light Driving Section

Item 项目	Symbol 符号	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Forward Voltage	V_F	-	3.1	-	V	Note1
Forward Current	I_F	-	120	-	mA	Note1
Backlight Power consumption	P_{BL}	-	0.372	-	Watt	Note1
LED life time	-	30000	-	-	Hours	Note2
LED Quantity			6		PCS	

(Ta=+25°C,GND=0V)

Note1:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_{LED}=20mA(Per Led). The LED life time could be decreased if operating I_{LED} is larger than 20mA.

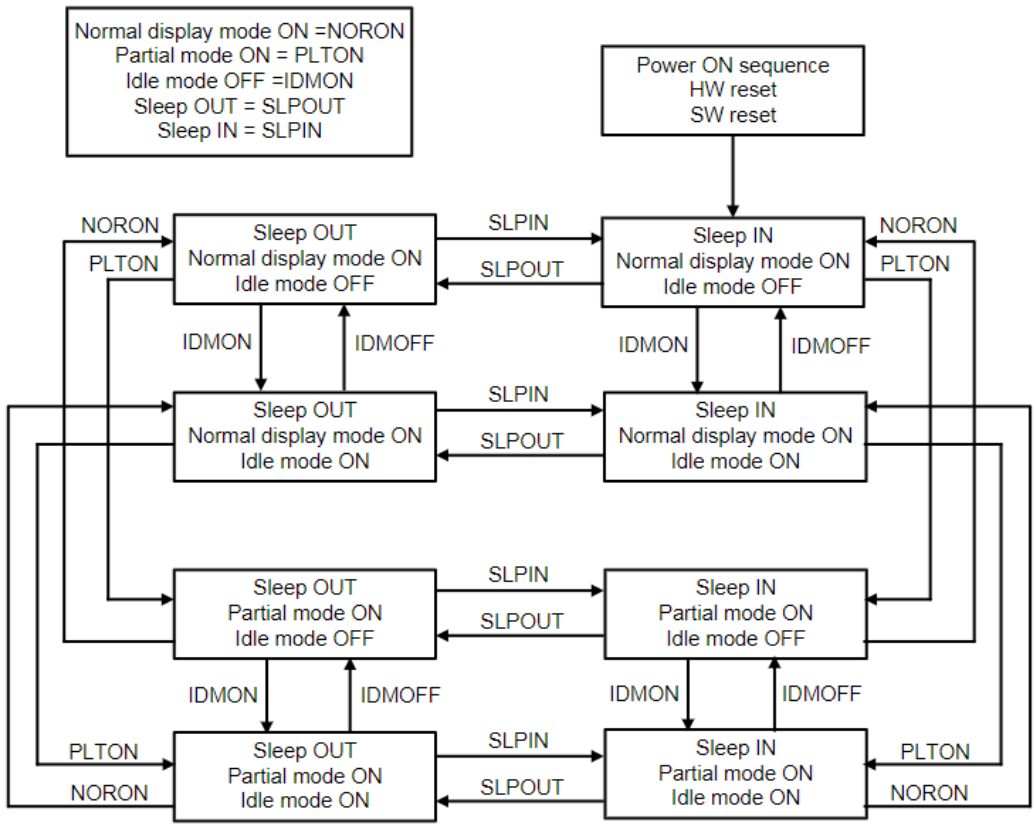
5.3 Power On/Off Sequence

5.3.1 LCM Power ON/OFF Sequence

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

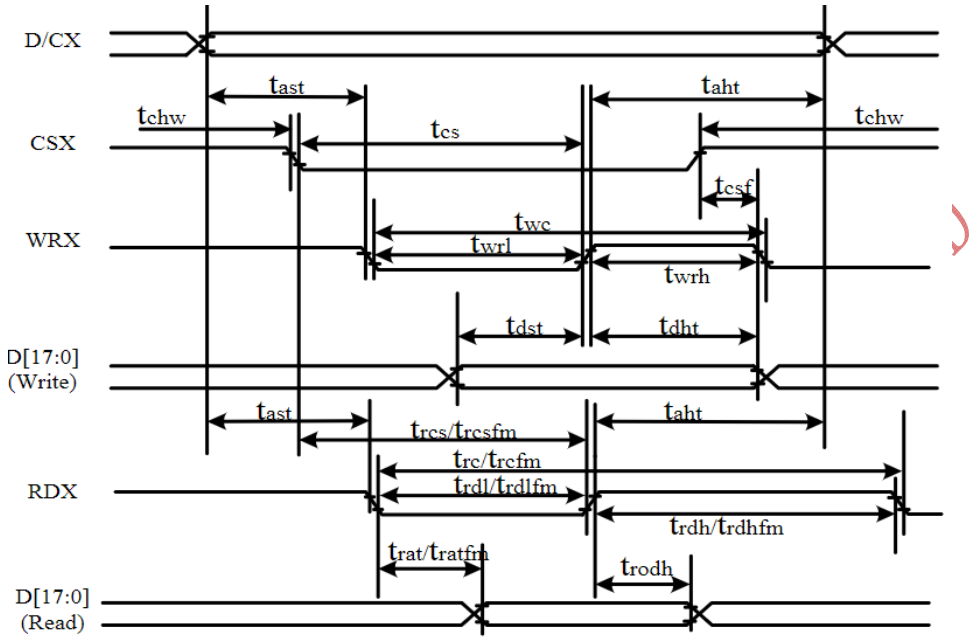


Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

5.4 AC Characteristics

5.4.1 Display Parallel 8/16-bit Interface Timing Characteristics

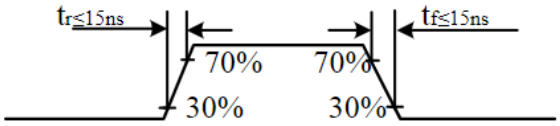


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	70	-	ns	
D[17:0],D[15:0],D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	

	tratfm	Read access time	-	340	ns
	trod	Read output disable time	20	80	ns

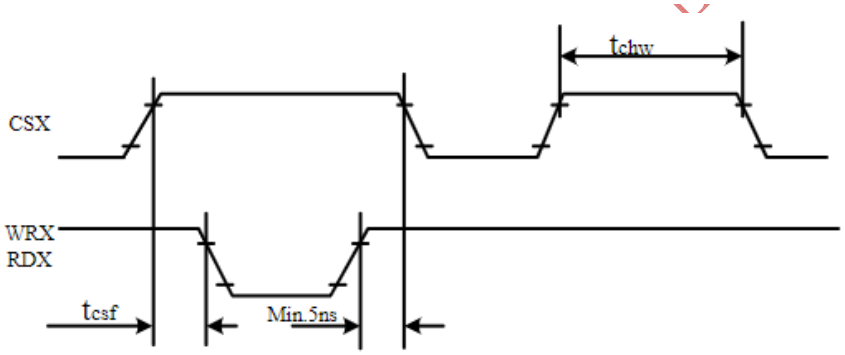
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

Figure91.



CSX timings :

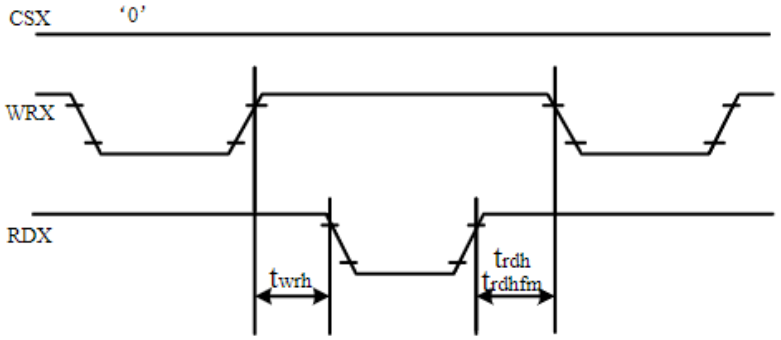
Figure92.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

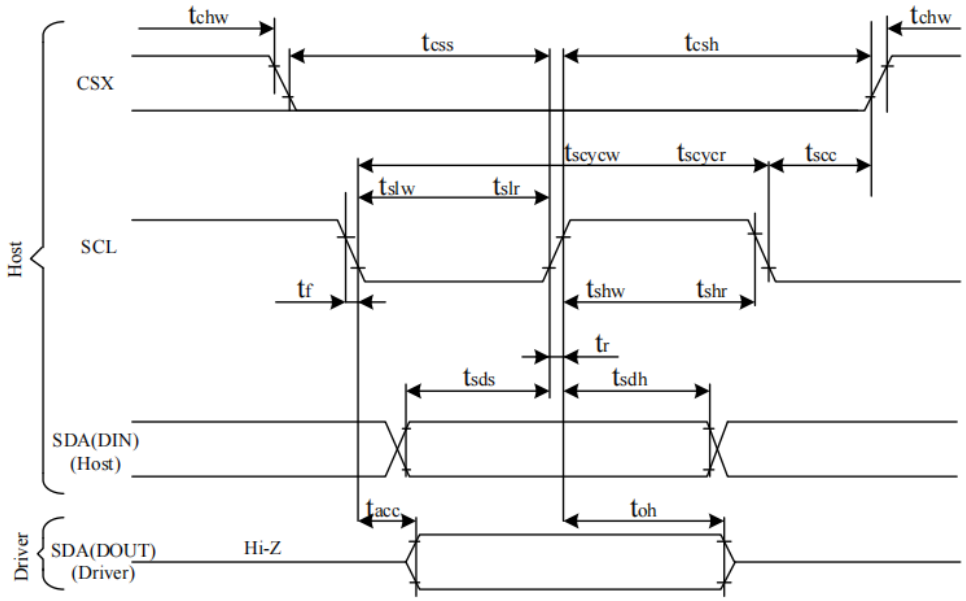
Write to read or read to write timings:

Figure92.



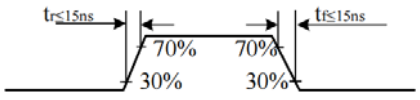
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

5.4.2 Display Serial Interface Timing Characteristics (3-line SPI system)

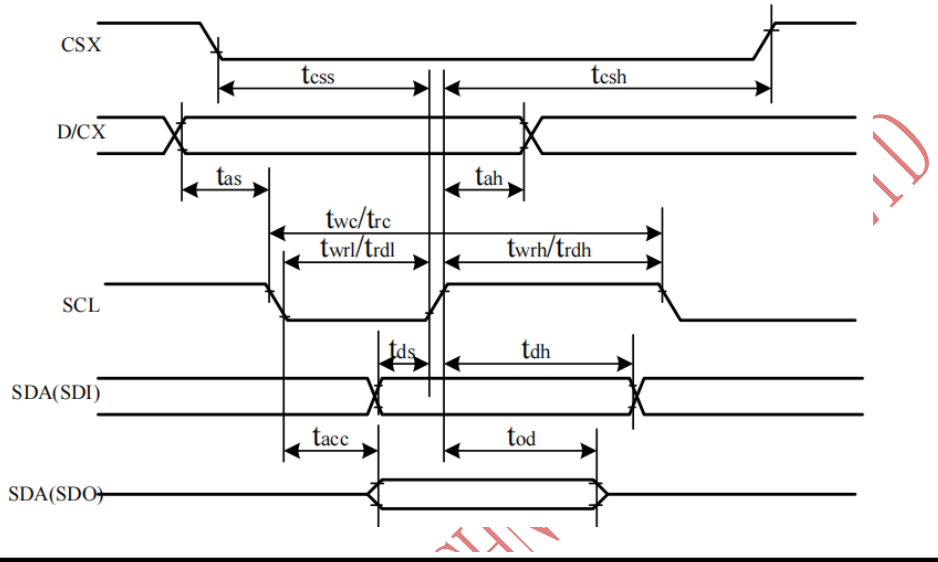


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
	tslw	SCL "L" Pulse Width (Write)	5	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	5	-	ns	
	tsdh	Data hold time (Write)	5	-	ns	
SDA/SD0(Outp)	tacc	Access time (Read)	10	-	ns	
CSX	tscc	SCL-CSX	10	-	ns	
	tchw	CSX "H" Pulse Width	10	-	ns	
	tcss	CSX-SCL Time	20	-	ns	
	tcsh		40	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSSA=VSSC=0V

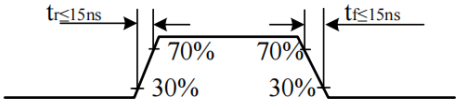


5.4.3 Display Serial Interface Timing Characteristics (4-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	20	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	5	-	ns	
	tdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



5.5 Timing Diagram

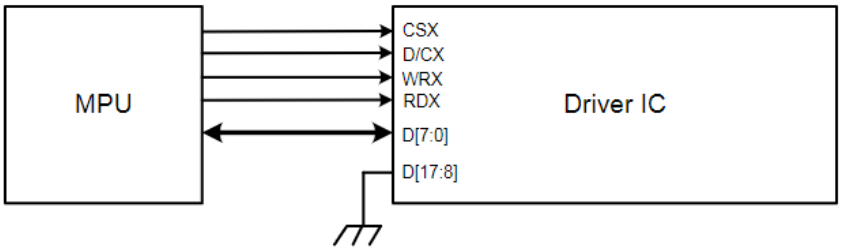
5.5.1 Timing Parameters

IM2	IM1	IM0	MCU-Interface	Pins in use	
				Register	GRAM
0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0]
1	0	1	3-wire 9-bit data serial interface I	SDA: In/OUT	
1	1	0	4-wire 8-bit data serial interface I	SDA: In/OUT	
1	0	0	3wires 24-bit data serial interface (ID0)	SDI, SDO, SCL, CSX	
1	1	1	3wires 24-bit data serial interface (ID1)	SDI, SDO, SCL, CSX	

MCU-8BIT

The 8080-Ⅰ system 8-bit parallel bus interface of GC9307 can be used by setting external pin as IM [3:0] to“0000”.The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure53.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Table 11.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

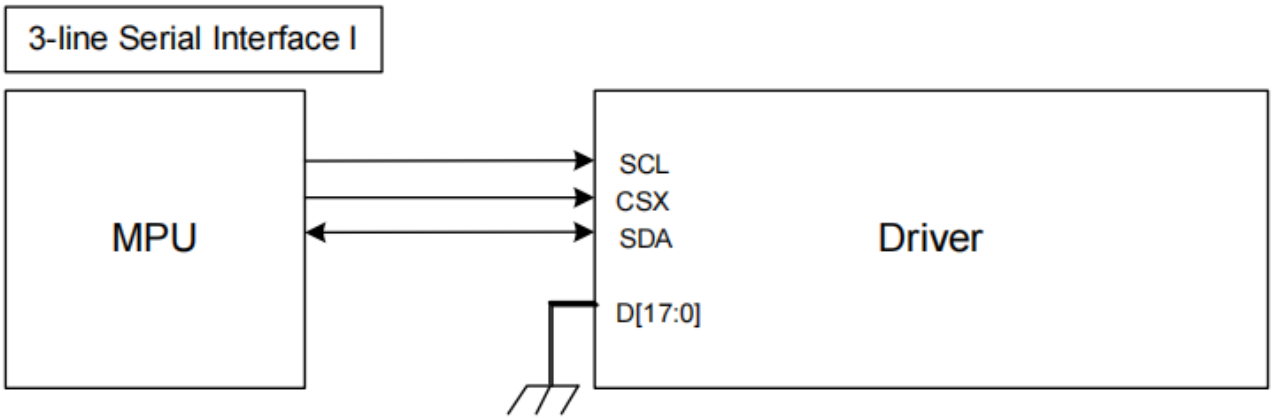
One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Table12.

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

3-WIRE 9-BIT DATA SERIAL INTERFACE I

The 3-line/9-bit serial bus interface of GC9307 can be used by setting external pin as IM [3:0] to “0101” for serial interface I or IM [3:0] to “1101” for serial interface II. The shown figure is the example of 3-line SPI interface.



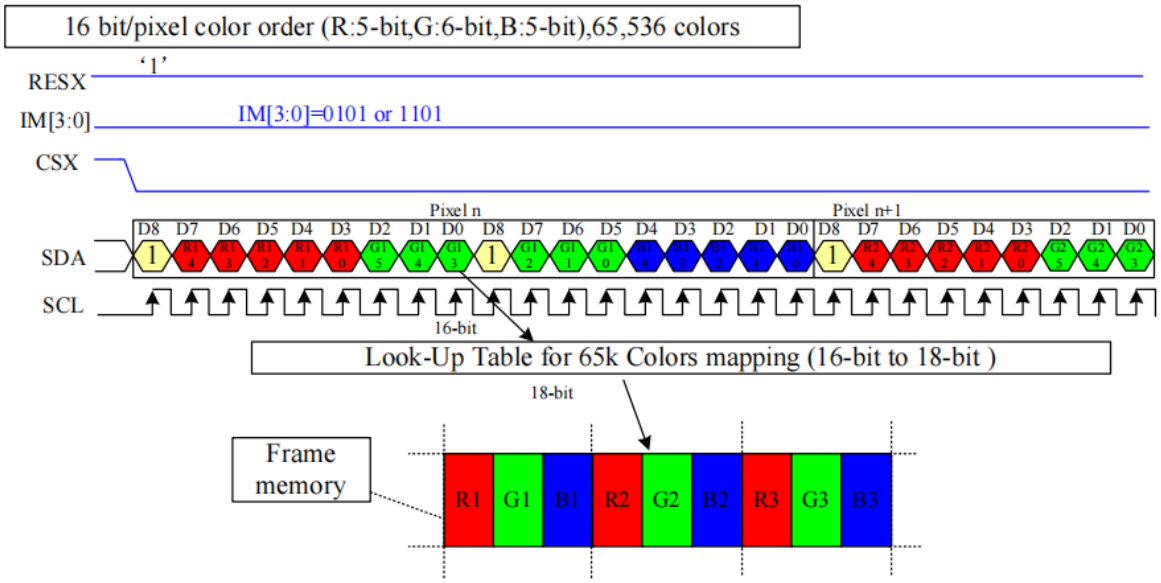
In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

Figure41.



Note 1: The pixel data with 16-bit color depth information.

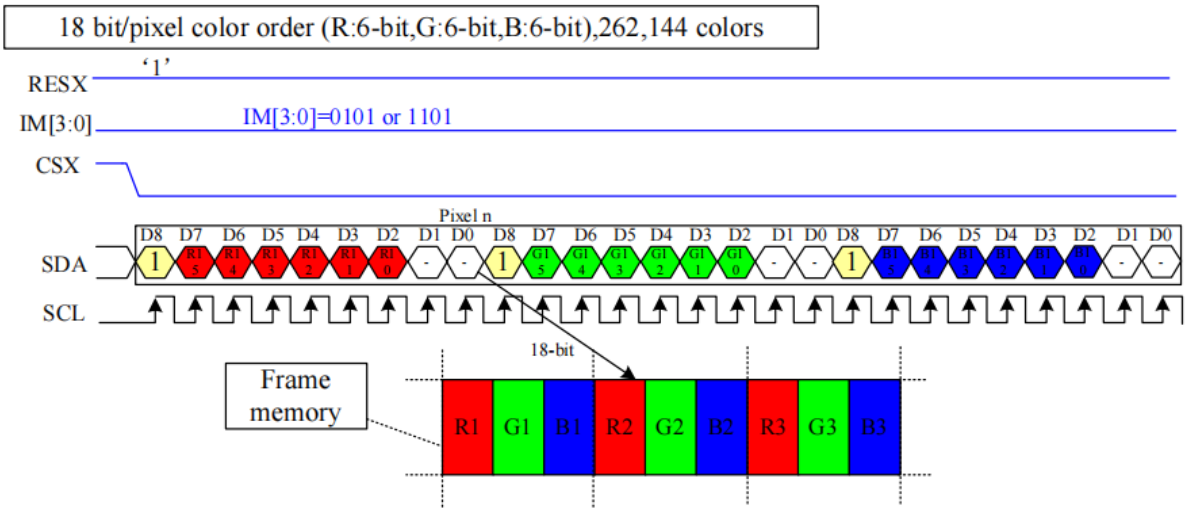
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

Figure42.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

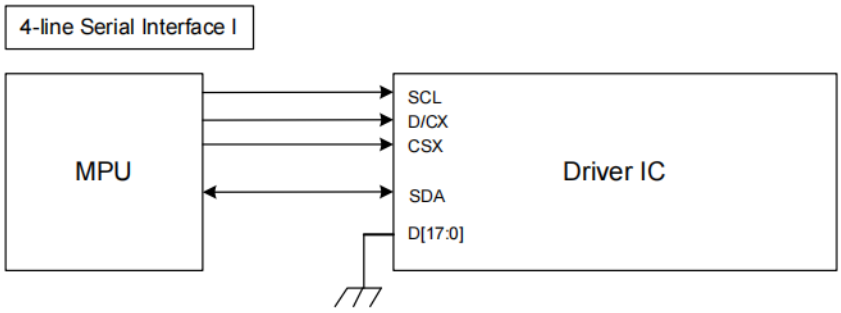
Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

4-WIRE 8-BIT DATA SERIAL INTERFACE I

The 4-line/8-bit serial bus interface of GC9307 can be used by setting external pin as IM [3:0] to “0110” for serial interface I or IM [3:0] to “1110” for serial interface II. The shown figure is the example of 4-line SPI interface.

Figure43.

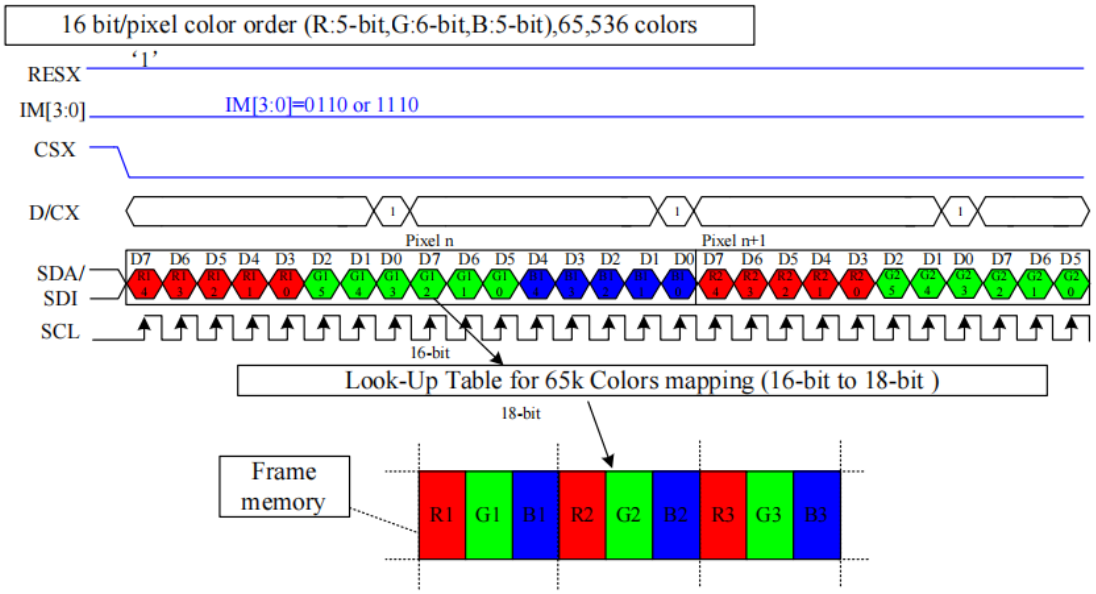


In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

Figure45.



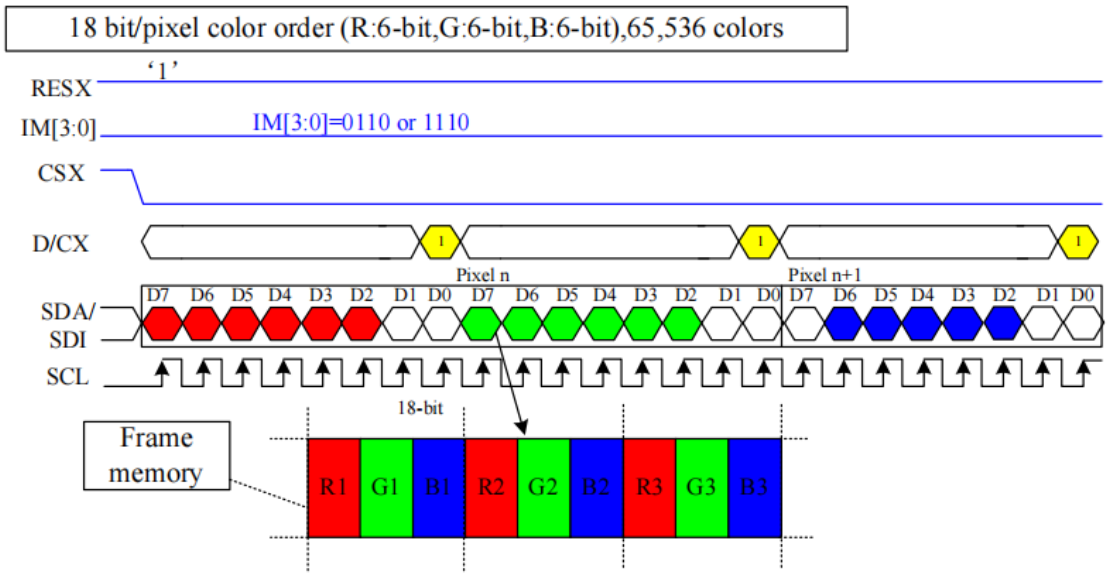
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure46.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

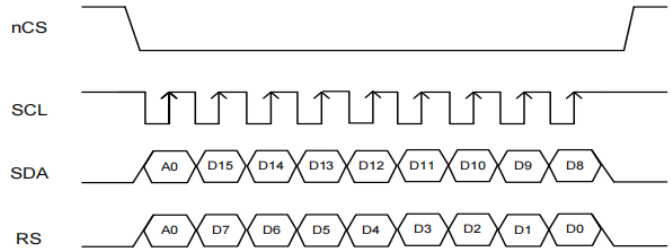
2-data-line mode

This mode is active when 2data_en (E9h[3]) set to “1” in 3-wire. Only frame pixle data write transitions are sent in 2-data-line mode, register write/read is still sent in 3-wire.

The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and DCX are serial data lines.

Serial data must be input to SDA in the sequence A0, D15 to D10 and DCX in the sequence A0, D7 to D0. The GC9307 reads the data at the rising edge of SCL signal. The first bit of serial data A0 is data/command flag. It must be set to "1", D15 to D0 bits are display RAM data.

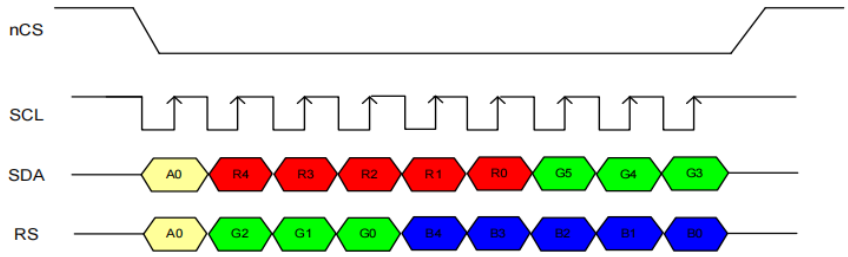
Figure47.



Five data formats are supported in 2-data-line mode, which is indicated by 2data_mdt (E9h[2:0]) .

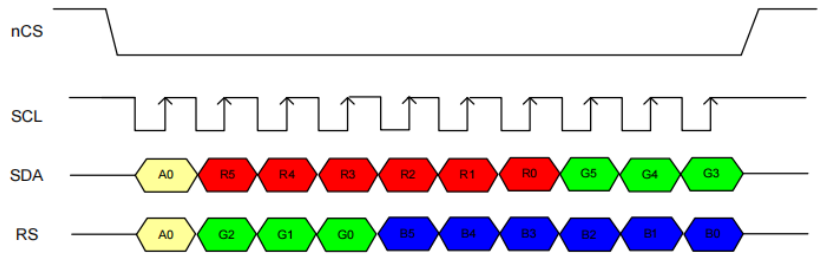
1)RGB565 1pixel/transition(65K color,2data_mdt[2:0]=’000’)

Figure48.

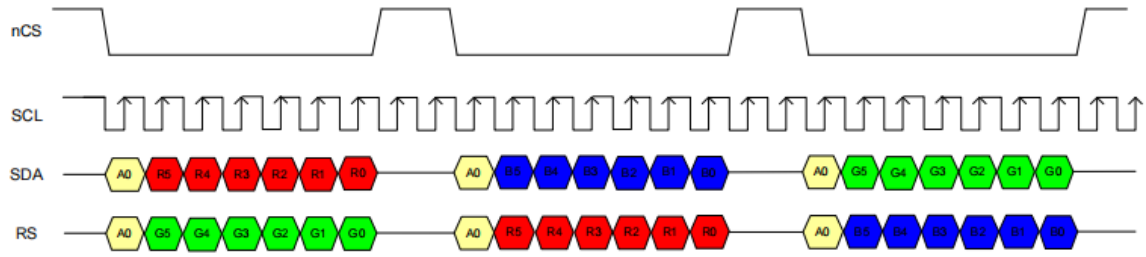


2)RGB666 1pixel/transition(262K color,2data_mdt[2:0]=’001’)

Figure49.

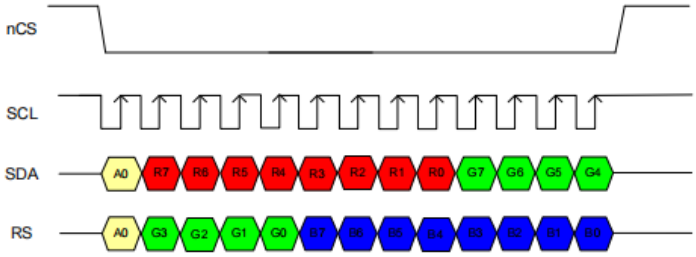


3)RGB666 2/3pixel/transition(262K color,2data_mdt[2:0]=’010’)



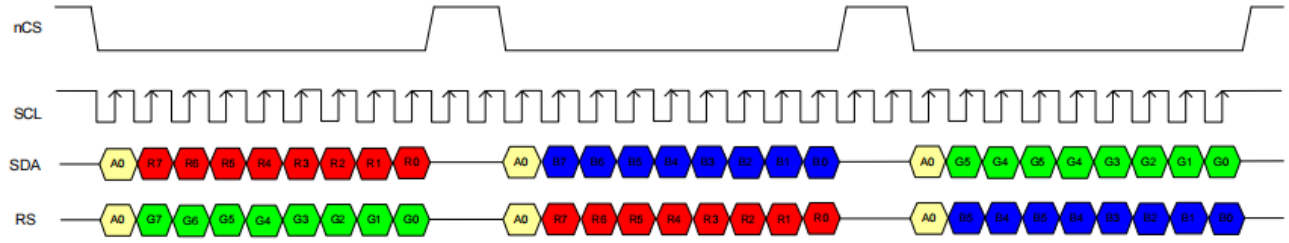
4)RGB888 1pixel/transition(4M color,2data_mdt[2:0]='100')

Figure51.



5)RGB888 2/3pixel/transition(4M color,2data_mdt[2:0]='110')

Figure52.



6. TP TIMING

Power on reset sequence

Reset should be pulled down to be low before powering on and powering down. I2C shouldn't be used by other devices during Reset time after VDD powering on (Trtp). INT signal will be sent to the host after ini- tializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 1ms.

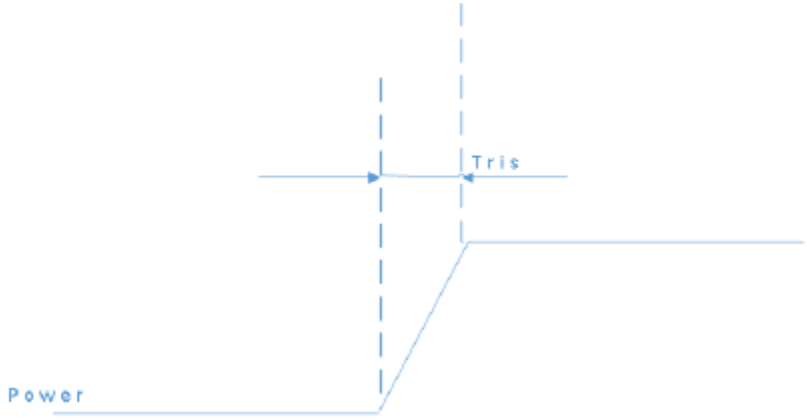


Figure 8.1 power on time

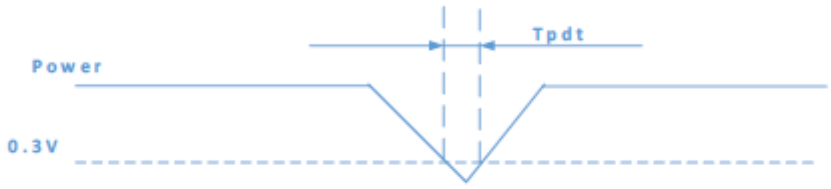


Figure 8-2 Power Cycle requirement

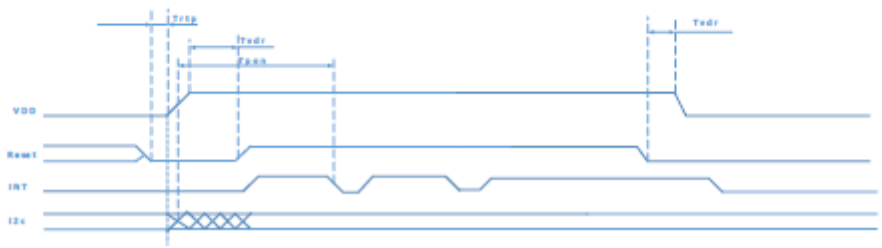


Figure 8-3 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

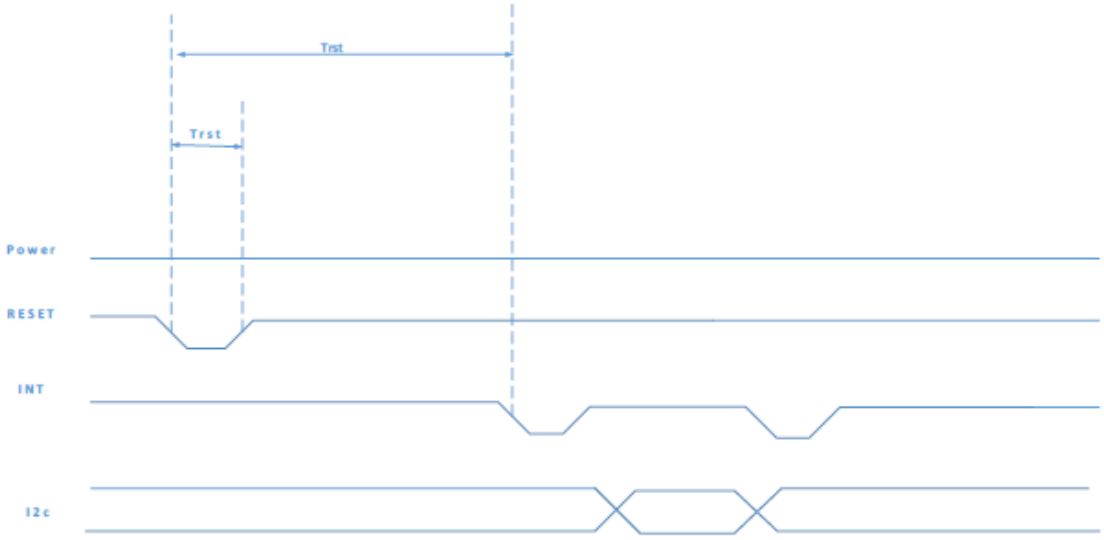


Figure 8.4 Reset Sequence

Table 8-1 Power on/Reset Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	2	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tpon	Time of starting to report point after powering on	--	200	ms
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	500	--	us

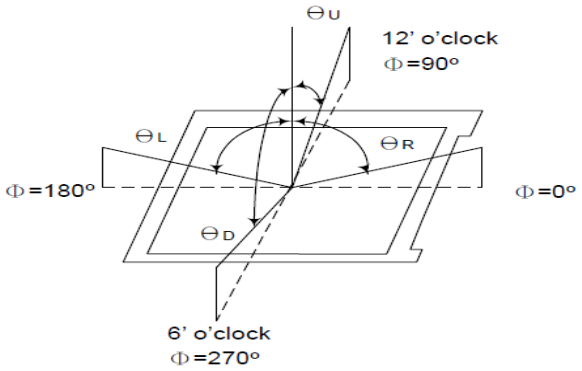
7. OPTICAL CHARACTERISTICS

Parameter 参数	Symbol 符号	Condition 条件	Min. 最小值	Typ. 典型值	Max. 最大值	Unit 单位	Remark 备注
Contrast Ratio	C/R	θ = 0°	1000	1200	-	-	Note(4)
NTSC Ratio	S	θ =0°	60	65		%	Note(7)
Luminance	L	θ =0°	300	350	-	cd/m2	Note(5)
Luminance uniformity	U_W	θ =0°	80		-	%	Note(3)
Response Time	T_R+ T_F	25 °C	-	30	35	ms	Note(2)
Color Coordination	W_X	θ =s 0° (Center) Normal viewing angle B/L On	-0.04	0.29	+0.04	NTSC (x,y)	Note(6)
	W_Y			0.30			
	R_X			0.656			
	R_Y			0.339			
	G_X			0.286			
	G_y			0.611			
	B_X			0.135			
	B_Y			0.144			
Viewing Angle	θ_L	C/R>10	75	80	-	Degree	Note(1)
	θ_R		75	80	-		
	θ_U		75	80	-		
	θ_D		75	80	-		

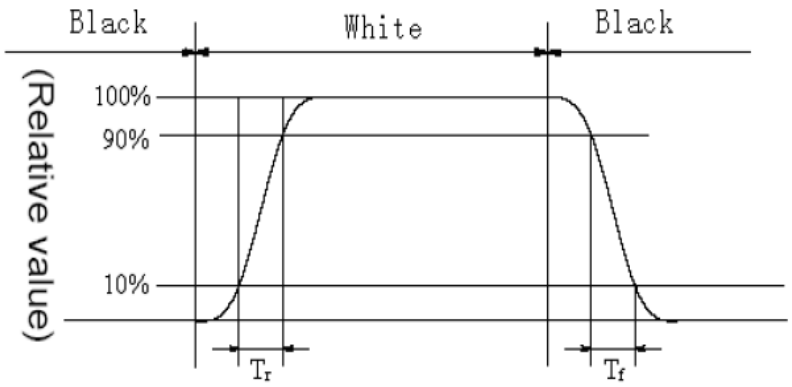
Test Conditions:

1. the ambient temperature is+25℃.
2. The test systems refer to Note 8.

Note1: Definition of Viewing Angle: The viewing angle range that the CR>10

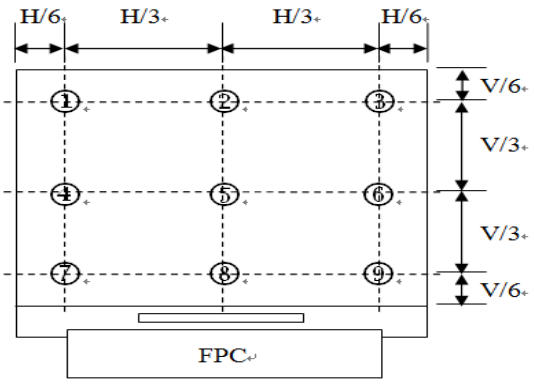


Note2: Definition of Response time: Sum of T_R and T_F



Note 3: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas, every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity} = \frac{\text{Luminance Uniformitv}}{\text{Luminance Uniformitv}} \times 100\%$$



Note4: Definition of Contrast Ratio (CR): measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

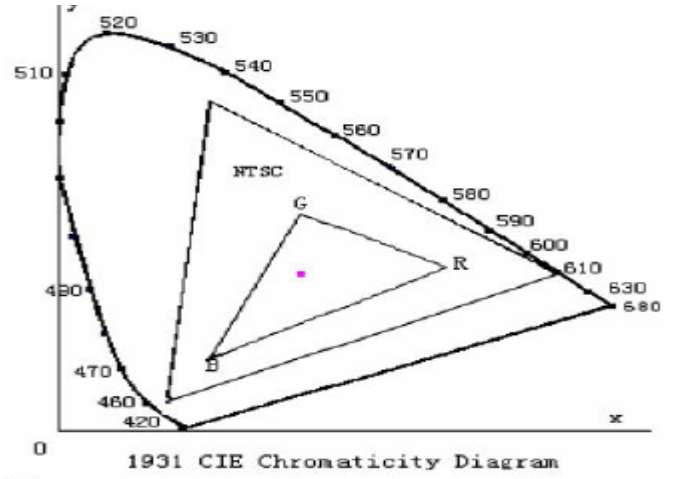
Note 5: Definition of Luminance: Center Luminance of white is defined as luminance values of 1point average across the LCD surface.

Note 6: Definition of Color Chromaticity (CIE 1931)

Color coordinates of white & red, green, blue measured at center point of LCD.

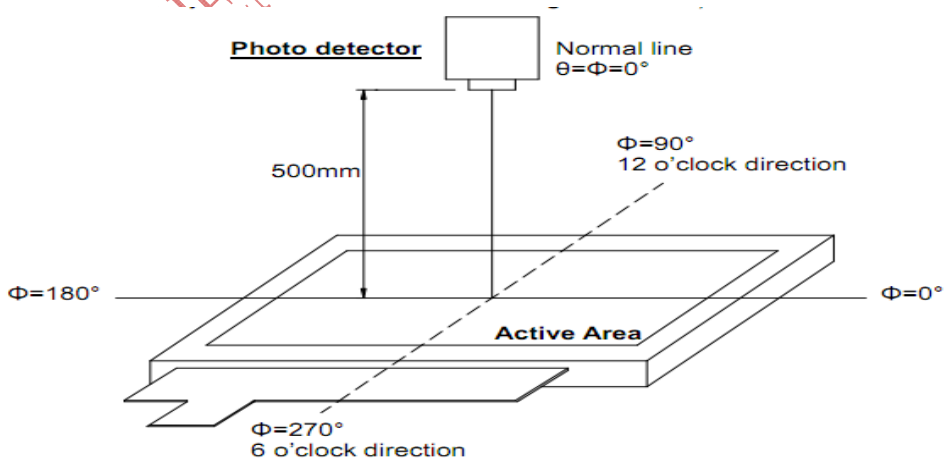
Note 7: Definition of NTSC ratio:

$$\text{NTSC ratio} = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}}$$



Note 8: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen.(Response time is measured by Photo detector TOPCON BM-7, Field of view: 1°/Height: 500mm.)



8. RELIABILITY

Item 项目	Test Condition 测试条件	Remark 备注
High Temperature Storage	Ta =+80°C / 96Hours	Note1,2,3
Low Temperature Storage	Ta =-30°C / 96Hours	Note1,2,3
High Temperature Operating	Ta =+70°C / 96Hours	Note1,2,3
Low Temperature Operating	Ta =-20°C / 96Hours	Note1,2,3
Temperature Cycle storage Test	-30°C/30min ⇆+80°C /30min for 30cycles,Transfer time less than 5min	Note2,3
Thermal humidity storage Test	60°C x 90%RH / 96Hours	Note2,3
ESD	C=150PF,R=330 Ohm Air:±8kv,5times(Center) Contact: ±4kv,5times(Center)	Note4

Inspection after Test:

Note1:Ta is the ambient temperature of samples.

Note 2: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but doesn't guarantee all the cosmetic specification.

Note 3: Before cosmetic and function tests , the product must have enough recovery time, at least 2 hours at room temperature.

9. PACKAGE DRAWING