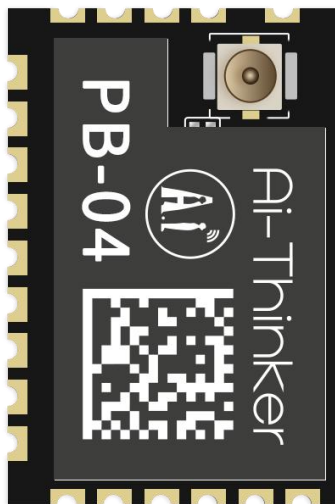


# PB-04 Specification

Version V1.0.0

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## Document Revision History

Version	Date	Created / Revised Content	Prepared by	Approved by
V1.0.0	2026-05-26	First edition	Wang Yeqing	Guan Ning

## Contents

1 Product Overview .....	5
1.1 Features .....	6
1.2 Application Scenarios .....	7
2 Key Specifications .....	8
3 Electrical Characteristics .....	9
3.1 Recommended Operating Conditions .....	9
3.2 I/O DC Electrical Characteristics .....	9
3.3 Electrostatic Discharge .....	9
3.4 BLE RF Performance .....	10
3.5 Power Consumption .....	10
4 Mechanical Specifications .....	11
4.1 Module Dimensions .....	11
4.2 External Antenna Connector Dimensions .....	11
5 Pin Definition .....	12
6 Schematic .....	14
7 Design Guide .....	15
7.1 Application Reference Circuit .....	15
7.2 Recommended PCB Footprint Dimensions .....	16
7.3 Antenna Layout Requirements .....	16
7.4 Power Supply .....	17
7.5 GPIO .....	17
8 Storage Conditions .....	18
9 Reflow Soldering Profile .....	18
10 Packaging Information .....	19
11 Contact Information .....	19
Disclaimer and Copyright Notice .....	20
Notice .....	20
Statement .....	21

## List of Figures

Figure 1	Main Chip Architecture Diagram .....	5
Figure 2	ESD Protection Symbol .....	9
Figure 3	Module Dimensions (Unit: mm) .....	11
Figure 4	External Antenna Connector Dimensions (Unit: mm) .....	11
Figure 5	Pin Diagram .....	12
Figure 6	Schematic .....	14
Figure 7	Application Reference Circuit .....	15
Figure 8	Recommended PCB Footprint Dimensions (Unit: mm) .....	16
Figure 9	Antenna Layout Diagram .....	16
Figure 10	DC-DC Buck Circuit .....	17
Figure 11	Level-shifting Circuit .....	17
Figure 12	Reflow Soldering Profile .....	18
Figure 13	Tape and Reel Packaging Diagram .....	19

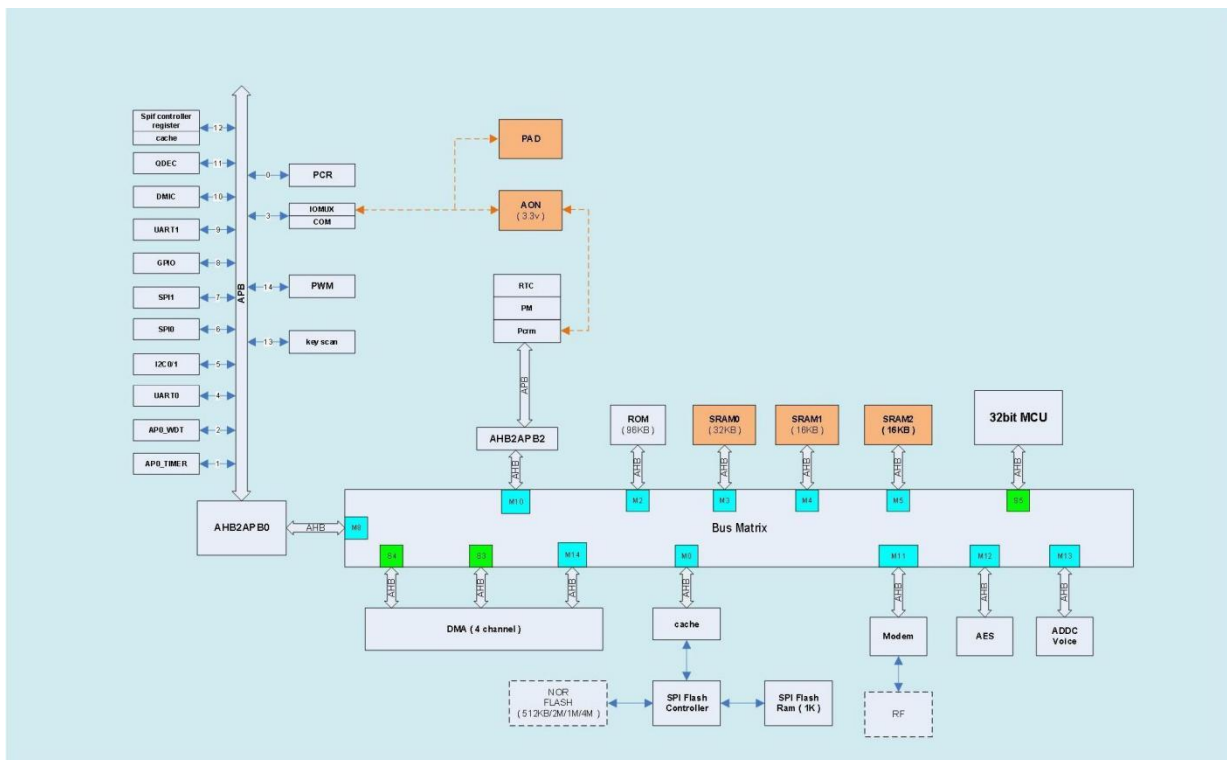
## List of Tables

Table 1	Key Specifications .....	8
Table 2	Recommended Operating Conditions .....	9
Table 3	I/O DC Electrical Characteristics .....	9
Table 4	BLE RF Performance .....	10
Table 5	Power Consumption .....	10
Table 6	Pin Function Definition .....	12

# 1 Product Overview

PB-04 is a Bluetooth module developed by Shenzhen Ai-Thinker Technology Co., Ltd. It utilizes the PHY6222 chip as its core processor. The PHY6222 supports BLE 5.4 and is equipped with a high-performance, low-power 32-bit processor, featuring ultra-low power consumption, high performance, and multi-mode radio capability. In addition, the PHY6222 supports Bluetooth Low Energy (BLE) with security, application, and over-the-air (OTA) download update.

The PB-04 module provides a rich set of peripheral interfaces, including SPI, UART, I2C, PWM, ADC, Timer, DMIC/AMIC, GPIO, and others. It can be widely applied in fields such as the Internet of Things (IoT), mobile devices, wearable electronics, and smart home systems.



**Figure 1 Main Chip Architecture Diagram**

## 1.1 Features

### Wireless

- Supports Bluetooth BLE 5.4 link controller
- -95dBm sensitivity @ 1Mbps GFSK
- -92dBm sensitivity @ 2Mbps GFSK
- TX Power -20 to +5dBm
- RSSI (1dB resolution)

### Microcontroller Subsystem

- High-performance, low-power 32-bit processor
- SWD interface

### Memory

- eFuse: 256 bit
- SRAM: 64KB
- Serial Flash: 128KB–8MB
- 96KB ROM

### Clock

- 16MHz & 32.768kHz external crystal oscillators

- 32MHz & 32.768kHz internal RC oscillators

### Security

- Supports AES-128 bit

### Software

- Compatible with Bluetooth 5.4
- Supported data rates: 1Mbps, 2Mbps (BLE)
- Supports SIG-Mesh multi-feature
- Supports OTA

### Peripherals

- Supports SPI, UART, I2C, PWM, ADC, GPIO, Timer, DMIC/AMIC, etc.

### Package Type

- Adopts SMD-20 package

### Development Environment

- Supports secondary development; integrated Windows development environment

## 1.2 Application Scenarios

- Smart Home
- Industrial Equipment Interaction
- Wearable Electronic Devices
- Internet of Things (IoT)
- Mobile Devices

## 2 Key Specifications

**Table 1 Key Specifications**

<b>Model</b>	PB-04
<b>Package</b>	SMD-20
<b>Dimensions</b>	13.9*9.0*2.8 (mm)
<b>Antenna Type</b>	External antenna (4th Gen I-PEX connector) / Castellated antenna
<b>Frequency Range</b>	2400–2483.5MHz
<b>Operating Temperature</b>	-40–105°C
<b>Storage Conditions</b>	-40–125°C, <90% RH
<b>Power Supply Range</b>	VDD: 1.8V–3.6V, supply current $\geq$ 100mA
<b>Supported Interfaces</b>	SPI, UART, I2C, PWM, ADC, Timer, SWD, DMIC/AMIC, GPIO, etc.
<b>Available I/Os</b>	13 (default)
<b>UART Baud Rate</b>	115200bps (default)
<b>Wi-Fi Security</b>	AES-128 encryption hardware
<b>Flash</b>	512KB (default), up to 8MB

### 3 Electrical Characteristics

#### 3.1 Recommended Operating Conditions

**Table 2 Recommended Operating Conditions**

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage	1.8	3.3	3.6	V
I	Supply Current	100	-	-	mA

#### 3.2 I/O DC Electrical Characteristics

**Table 3 I/O DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit
VIH	High-level Input Voltage	2.4	-	-	V
VIL	Low-level Input Voltage	-	-	0.5	V
VOH	High-level Output Voltage	2.5	-	-	V
VOL	Low-level Output Voltage	-	-	0.5	V
I <sub>max</sub>	I/O Maximum Operating Current	-	-	10	mA

#### 3.3 Electrostatic Discharge

The PB-04 is an ESD-sensitive device and requires special precautions during handling.



**Figure 2 ESD Protection Symbol**

### 3.4 BLE RF Performance

**Table 4 BLE RF Performance**

Description	Typ			Unit
Frequency Range	2400–2483.5			MHz
<b>Output Power</b>				
Data Rate Mode	Min	Typ	Max	Unit
1Mbps	-	5	-	dBm
2Mbps	-	5	-	dBm
<b>Receiver Sensitivity</b>				
Data Rate Mode	Min	Typ	Max	Unit
1Mbps Sensitivity @ 30.8% PER	-	-95	-	dBm
2Mbps Sensitivity @ 30.8% PER	-	-92	-	dBm

### 3.5 Power Consumption

The following power consumption data are measured based on a 3.3V power supply and an ambient temperature of 25°C.

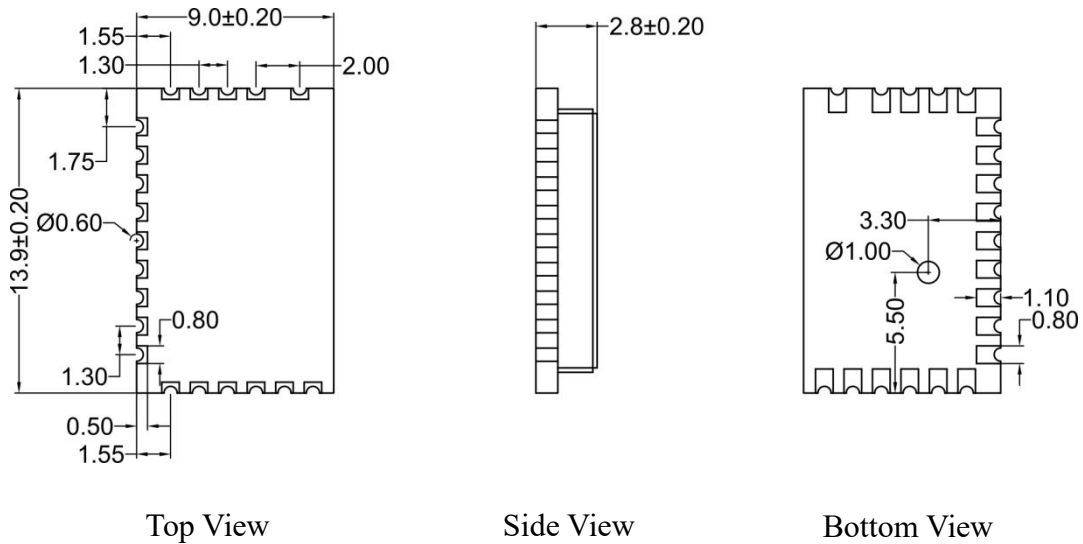
- The POUT power for all transmit modes is measured at the antenna interface.
- All transmission data are measured at 100% duty cycle in continuous transmit mode.

**Table 5 Power Consumption**

Mode	Min	Avg	Max	Unit
TX PHY=1M, PRBS9, Pout = 5dBm	-	9	-	mA
TX PHY=2M, PRBS9, Pout = 5dBm	-	6	-	mA
RX PHY= 1M, Packet Length 1024 bytes	-	6	-	mA
RX PHY= 2M, Packet Length 1024 bytes	-	6	-	mA

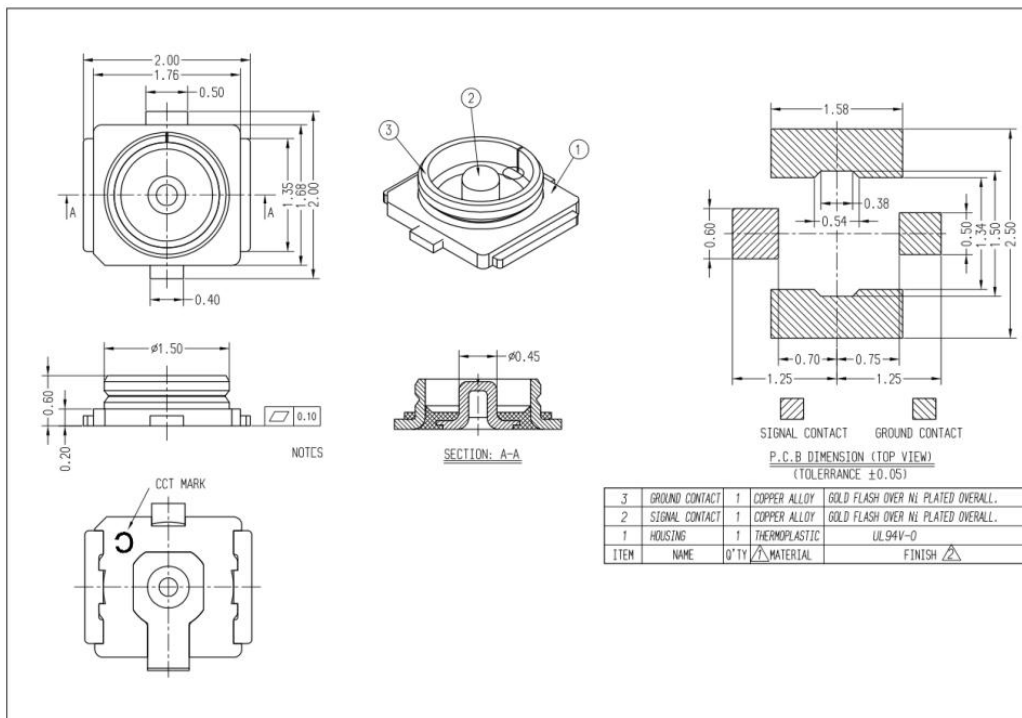
## 4 Mechanical Specifications

### 4.1 Module Dimensions



**Figure 3 Module Dimensions (Unit: mm)**

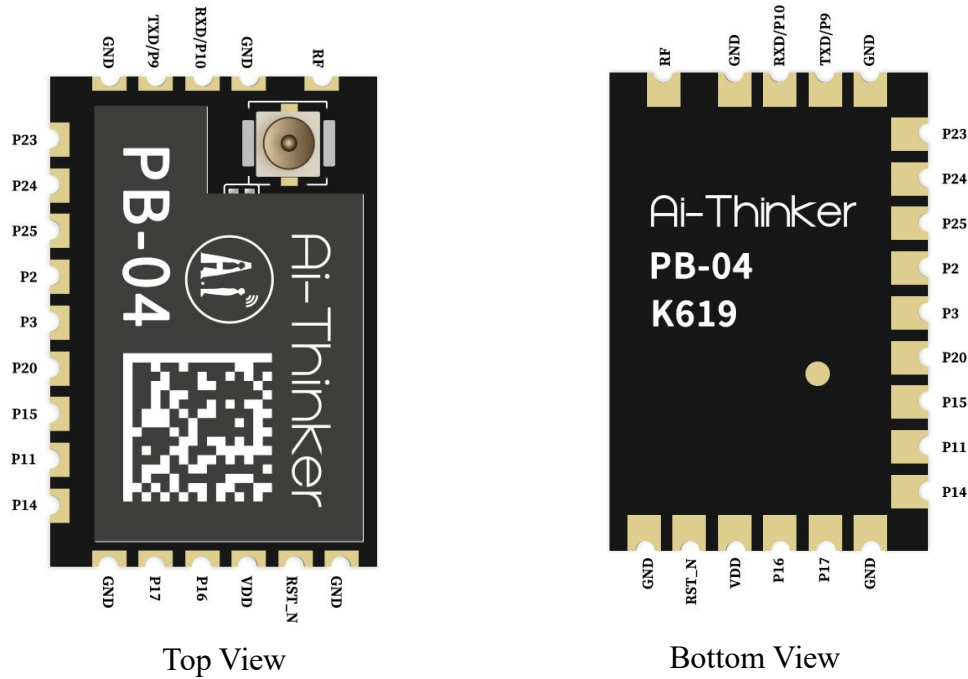
### 4.2 External Antenna Connector Dimensions



**Figure 4 External Antenna Connector Dimensions (Unit: mm)**

## 5 Pin Definition

The PB-04 module exposes a total of 20 pins, as shown in the pin diagram. The pin function definition table provides the detailed interface specifications.



**Figure 5 Pin Diagram**

**Table 6 Pin Function Definition**

No.	Name	Function
1	GND	Ground
2	RXD / P10	RXD / GPIO 10
3	TXD / P9	TXD / GPIO 9
4	GND	Ground
5	P23	GPIO 23 / ADC input 1 / Micbias output reference
6	P24	GPIO 24 / ADC input 2
7	P25	GPIO 25 / ADC Input 8
8	P2	GPIO 2 / SWD debug data input / output port
9	P3	GPIO 3 / SWD debug clock port
10	P20	GPIO 20 / ADC input 9 / PGA positive input
11	P15	GPIO 15 / ADC input 4 / Micbias output

12	P11	GPIO 11 / ADC input 0
13	P14	GPIO 14 / ADC input 3
14	GND	Ground
15	P17	GPIO17 / 32.768kHz crystal output
16	P16	GPIO16 / 32.768kHz crystal input
17	VDD	3.3V power supply
18	RST_N	Reset, active low
19	GND	Ground
20	RF	RF antenna
-	TM	Test mode enable

Note: 1. The bottom test point is the TM pin, which serves as Test Mode Enable. When TM is pulled high and RST\_N is reset, the module enters download mode. If TM is high at the moment of power-on, the module enters programming mode; if TM is low at the moment of power-on, the module boots normally.

## 6 Schematic

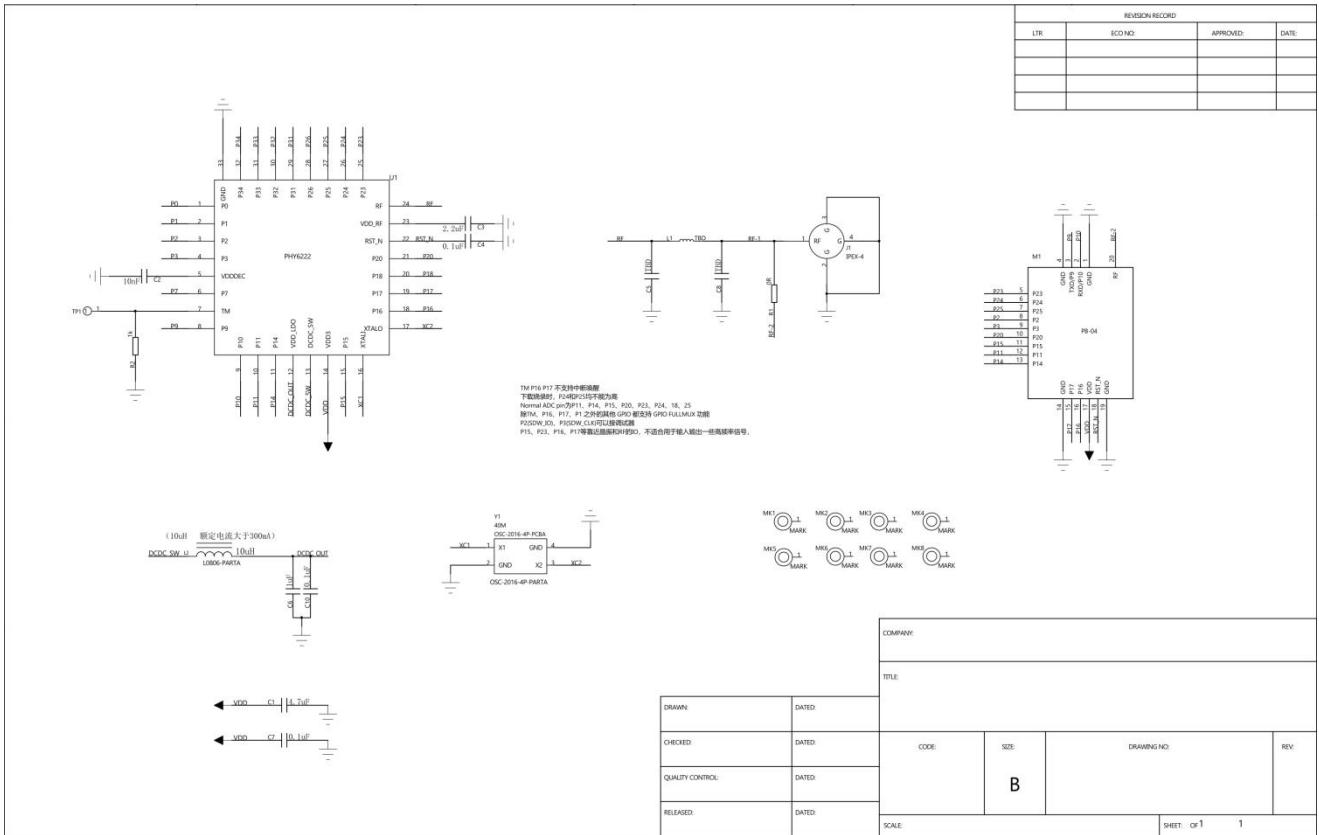
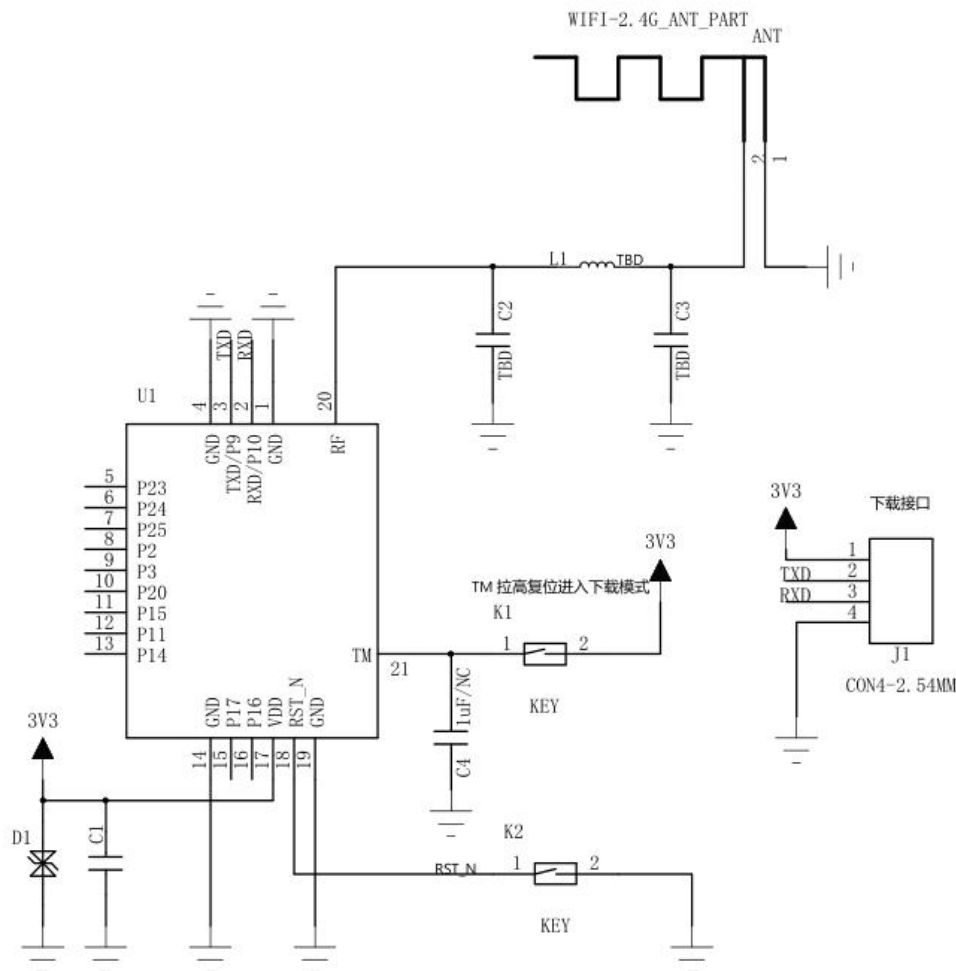


Figure 6 Schematic

## 7 Design Guide

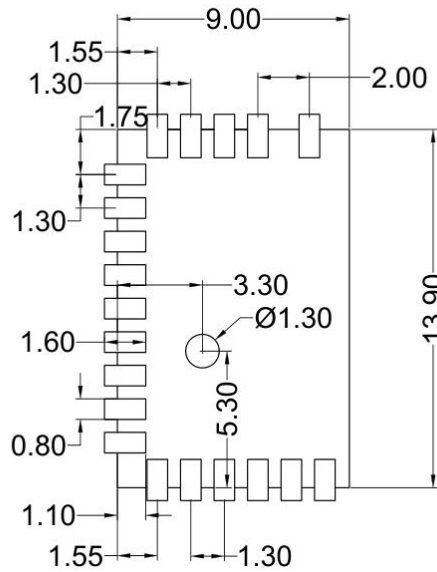
### 7.1 Application Reference Circuit



**Figure 7 Application Reference Circuit**

- The RF port on the mainboard shall reserve a  $\pi$ -type matching circuit.
- The bottom test point is the TM pin, which serves as Test Mode Enable. When TM is pulled high and RST\_N is reset, the module enters download mode. If TM is high at the moment of power-on, the module enters programming mode; if TM is low at the moment of power-on, the module boots normally.
- TXD and RXD are the module download ports.
- VDD supply voltage: 1.8–3.6V. The external power supply output current is recommended to be above 100mA.

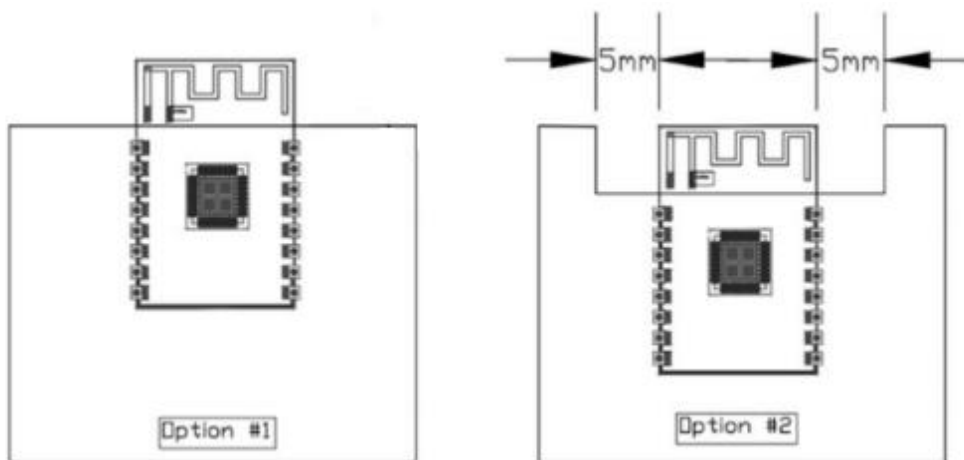
## 7.2 Recommended PCB Footprint Dimensions



**Figure 8 Recommended PCB Footprint Dimensions (Unit: mm)**

## 7.3 Antenna Layout Requirements

- For the installation position on the mainboard, the following 2 options are recommended.  
Option 1: Place the module at the mainboard edge, with the antenna area extending beyond it.  
Option 2: Place the module at the mainboard edge, with a clearance cutout at the antenna position.
- To ensure optimal antenna performance, metal components should be kept away from the antenna area, and the antenna should be placed as far as possible from high-frequency devices.



**Figure 9 Antenna Layout Diagram**

## 7.4 Power Supply

- VDD is recommended as 3.3V, with a peak current above 100mA.
- An LDO is recommended for power supply; if using DC-DC, the ripple should be controlled within 30mV.
- For the DC-DC power supply circuit, it is recommended to reserve space for dynamic response capacitors to optimize output ripple under large load transients.
- It is recommended to add ESD protection devices to the power interface.

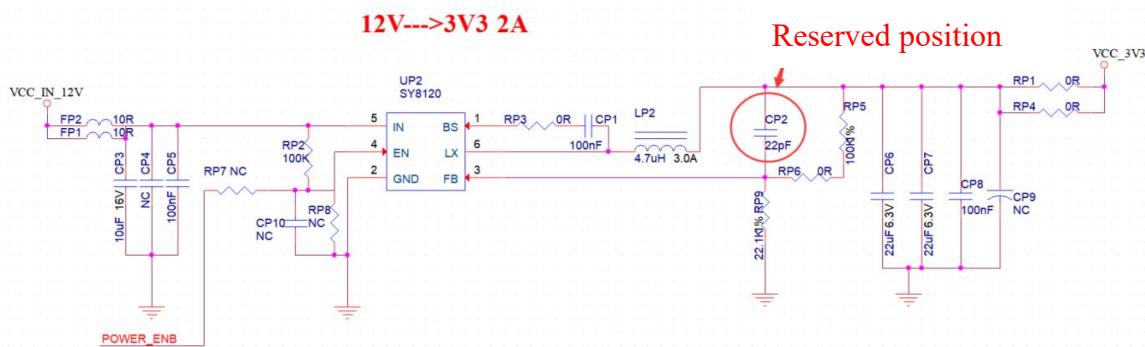


Figure 10 DC-DC Buck Circuit

## 7.5 GPIO

- Some I/O pins are exposed on the module periphery. To use these I/O pins, it is recommended to connect a 10-100Ω resistor in series with each I/O pin. This helps suppress overshoot, stabilize signal levels, and benefits both EMI and ESD protection.
- The pull-up or pull-down configuration for special I/O pins must follow the guidelines in the specification, as it affects the module's boot configuration.
- The module's I/O pins operate at 3.3V. If the I/O voltage level of the main controller and the module do not match, a level-shifting circuit must be added.
- If an I/O pin is directly connected to a peripheral interface or pin headers, it is recommended to reserve space for an ESD protection device near the connector on the I/O trace.



Figure 11 Level-shifting Circuit

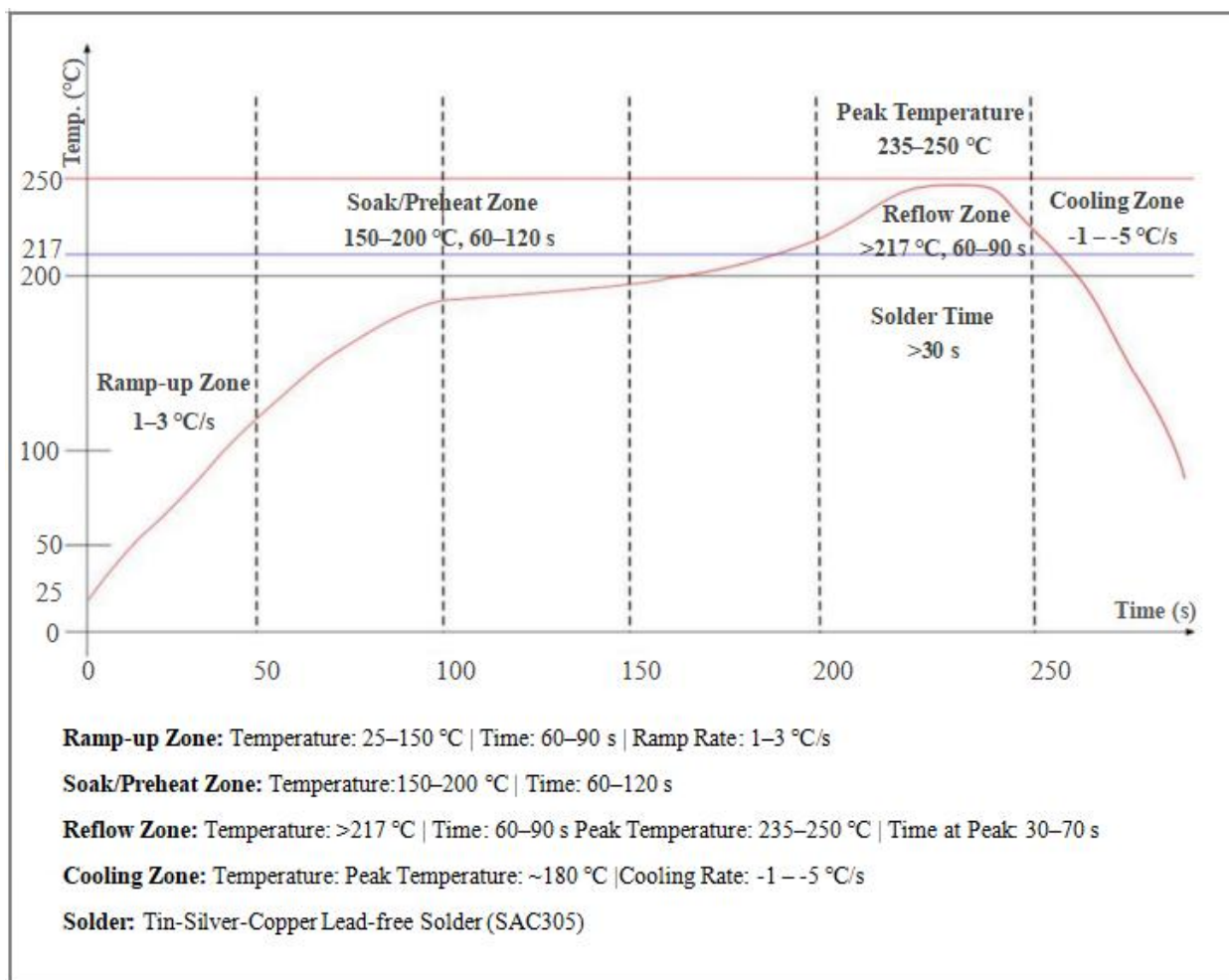
## 8 Storage Conditions

Products sealed in moisture barrier bags should be stored in a non-condensing atmosphere at  $< 40^{\circ}\text{C}$  and  $< 90\% \text{ RH}$ .

The moisture sensitivity level (MSL) of the module is level 3.

The module must be used within 168 hours after vacuum bag removal under conditions of  $25\pm 5^{\circ}\text{C}$  and  $60\% \text{ RH}$ . Otherwise, the module requires baking before being returned to production.

## 9 Reflow Soldering Profile



**Figure 12 Reflow Soldering Profile**

## 10 Packaging Information

The PB-04 module is packaged in tape-and-reel, 1200 pcs/reel.



Figure 13 Tape and Reel Packaging Diagram

## 11 Contact Information

[Official Website](#)

[Official Forum](#)

[Development DOCS](#)

[LinkedIn](#)

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[Taobao Store](#)

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