Data Sheet

BL616CL DataSheet

Mar. 2026

Features

- Wireless
  - 2.4 GHz RF transceiver
  - Wi-Fi 6 (IEEE 802.11 b/g/n/ax)
  - Bluetooth® 5.3
  - Wi-Fi Fast connection with BLE assistance
  - Wi-Fi/BLE Coexistence
  - Wi-Fi Security WPS/WEP/WPA/WPA2/WPA3
  - Wi-Fi 20MHz BW, 1T1R
  - Support LDPC, STBC, Beamformee, DL/UL OFDMA, MU-MIMO, TWT (Target Wake Time), SR(Spatial Reuse), DCM (Dual Carrier Modulation), ER (Extended Range)
  - Support Aggregation (AMPDU, AMSDU), Immediate Block Ack, Fragmentation and Defragmentation
  - Support RX diversity
  - Support IEEE 802.11e QoS WMM (Wi-Fi MultiMedia), IEEE 802.11w PMF (Protected Management Frames)
  - STA, SoftAP, STA+SoftAP and sniffer modes
  - Integrated RF balun, PA/LNA
  - Support External PA/LNA
- Microcontroller
  - 32-bit RISC-V CPU with FPU and DSP
  - Dynamic Frequency from 1MHz to 320MHz
  - Support RISC-V RV32IMAFCP instruction set
  - 16KB instruction cache, two-way set associative structure
  - 8KB data cache, two-way set associative structure
  - Support NOR FLASH XIP
- Audio Codec
  - Digital Microphone PDM Input
  - Audio PWM Output
- Memory
  - 388KB SRAM
    - 224K OCRAM
    - 160K WRAM
    - 4K HBN RAM
  - Embedded 2/4/8MB Flash (Optional)
  - Embedded 4/8MB pSRAM (Optional)
- Video/Image
  - Camera Sensor DVP interface
  - MJPEG encoder and decoder(optional)
  - LCD Display (QSPI, DBI)
- Security
  - Secure boot(support firmware encrypt & sign)
  - Secure debug
  - Support Anti-Rollback
  - XIP On-The-Fly AES Decryption (OTFAD)

  - Support TrustZone
  - AES-ECB/CBC/CTR/GMAC/XTS modes
  - MD5、SHA-1/224/256/384/512
  - TRNG (True Random Number Generator)
  - PKA (Public Key Accelerator) for RSA/ECC
  - 1024 bits eFuse
- Peripherals
  - USB 2.0 HS OTG (High-Speed 480Mb/s)
  - SDIO 2.0 slave
  - SD-card interface
  - 1 EMAC，support 10/100M
  - 1 DMA(8 channels)
  - 3 UART(partially supports 5V IO)
  - 2 I2C , support host mode
  - 2 SPI master/slave
  - 1 I2S master/slave
  - 1 PWM (4 channels with complementary outputs)
  - 2 GPTimer
  - 2 Watchdog
  - 1 12-bit~16-bit General-Purpose ADC(12 channels)
  - 1 touch(optional)
  - 1 PEC (Peripherals Expander Controller) , expandable peripherals including but not limited:
    - UART
    - I2C
    - SPI
    - GPIO
    - JTAG
    - DPI
    - DBI
    - PWM
    - IR
  - Flexible 37 (QFN48) or 29 (QFN40) or 21 (QFN32) GPIOs
- Power Modes
  - Stop
    - CPU WFI, peripheral clock stop (configurable), wireless off
  - Power Down Sleep
    - Support PDS1/3/7/11/15
    - Wireless/Peripheral/CPU can be selectively turned off
    - Support 384K RAM for retention
    - Support Peripheral/RTC/GPIO wake-up
    - Support Watchdog
  - Hibernate
    - Support 4K RAM for retention
    - Support RTC/GPIO wake-up
    - Support Watchdog
  - Shutdown
- Clock

  - Support external 24/26/32/40MHz crystal oscillator (XTAL)
  - Support external 32.768KHz crystal oscillator(XTAL32K)
  - Support Internal RC 32KHz oscillator(RC32K)
  - Support Internal RC Multi-Speed Main oscillator(RCM),frequency Support 8/16/32M
- Package Type
  - QFN32
  - QFN40
  - QFN48

Contents

1 Overview

BL616CL is Wi-Fi 6 + BLE 5.3 combo chipset for ultra-low power applications. It mainly includes two sub-systems, wireless and microcontroller.

Wireless subsystem contains 2.4G radio, Wi-Fi 802.11b/g/n/ax, and BLE baseband/MAC designs.

Microcontroller subsystem contains a low-power 32-bit RISC-V CPU with floating point units, DSP units, highspeed cache and memories. The maximum clock frequency can reach 320M.

Peripheral interfaces include Audio Codec, USB2.0, EMAC, Camera, Display (DBI), MJPEG, SDIO2.0, SD/MMC (SDH), Security Engine, SPI, UART, I2C, I2S, PWM, Timer, GPADC, etc., making it applicable in fields such as smart IoT, audio and video, and new energy.

The power management unit controls low-power modes, supporting PDS (Power Down Sleep, PDS1/3/7/15) and HBN (Hibernate) modes, with multiple wake-up sources to meet various low-power scenarios.

BL616CL supports secure boot, image encryption and signing, and firmware anti-rollback, meeting various security application requirements in IoT and new energy fields.

The system function block diagram is shown below.

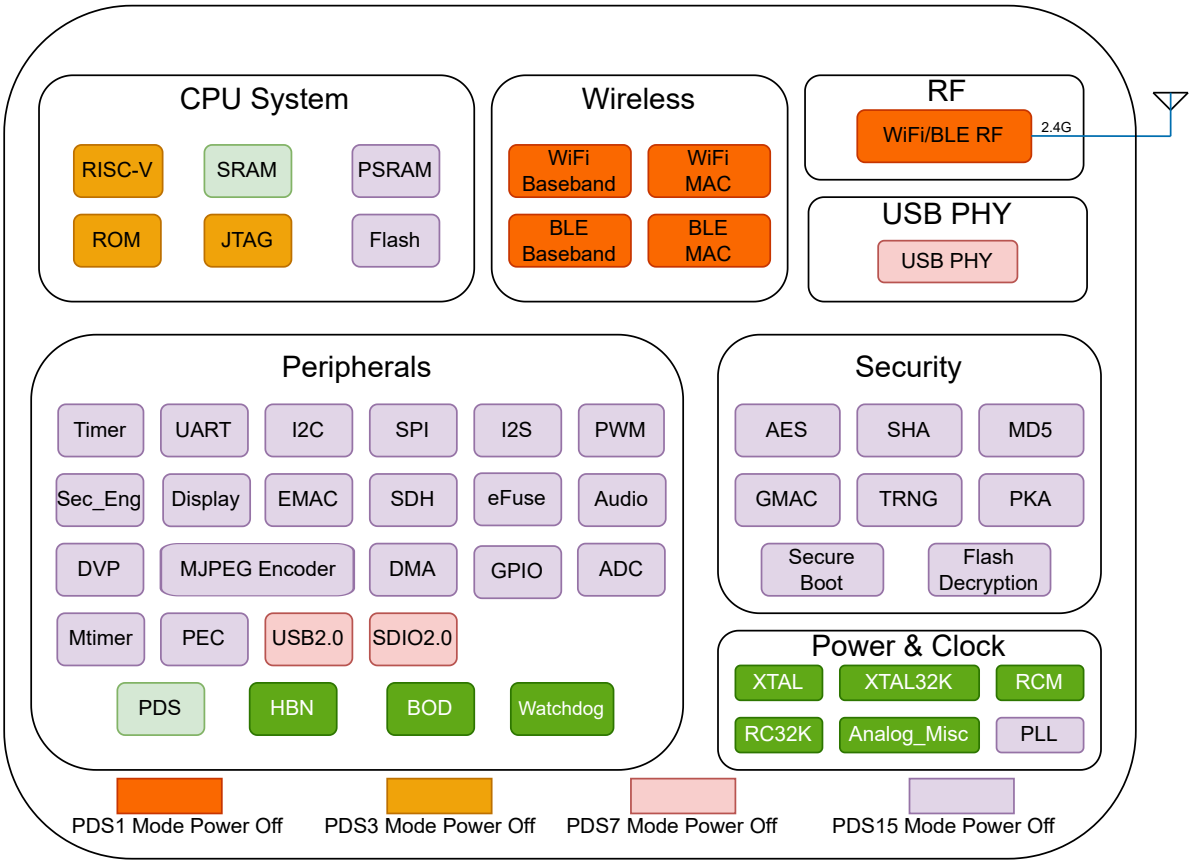


Fig. 1.1: BL616CL Functional Block Diagram

2 Functional Description

The system architecture is as follows:

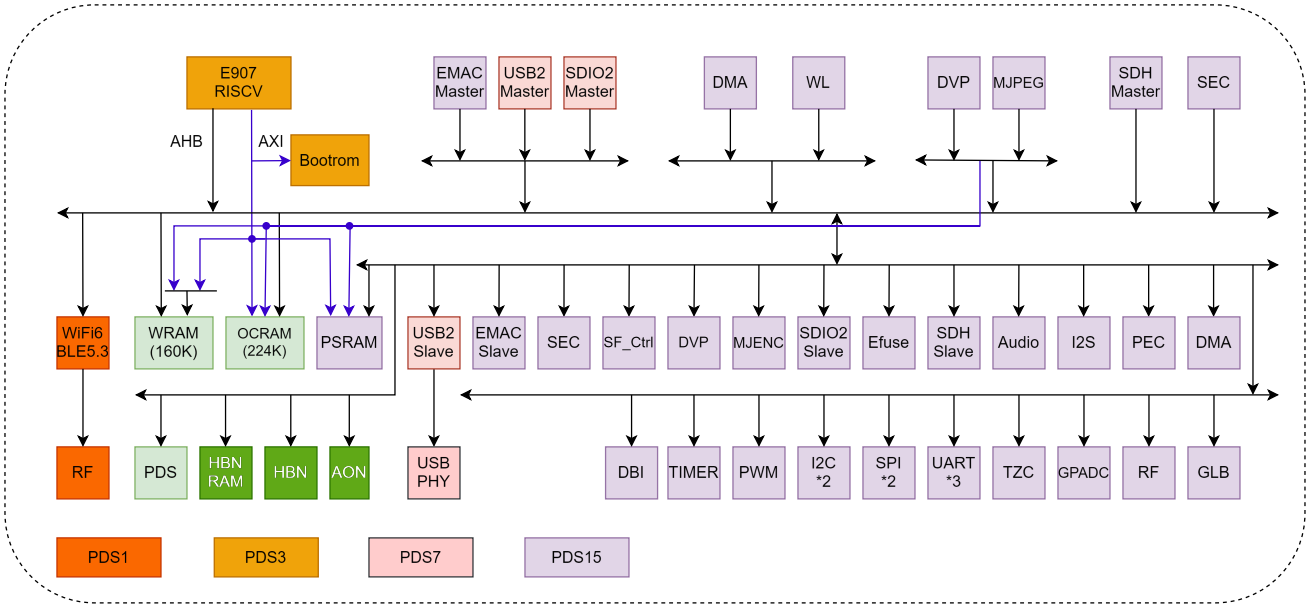


Fig. 2.1: BL616CL System Architecture Diagram

The CPU has two buses, AXI and AHB. ROM, OCRAM , and PSRAM are hung on the AXI bus to achieve high-speed access to these memory units. Each peripheral is connected to the CPU through the AHB bus.

2.1 CPU

BL616CL has a built-in 32-bit RISC-V CPU, which adopts a 5-stage pipeline structure: fetch, decode, execute, memory access, write back, support RISC-V 32/16-bit mixed instruction set, including 67 external interrupt sources, there are 4 bits that can be used to configure the interrupt priority.

2.2 Cache

The cache of BL616CL improves the performance of CPU accessing external memory, including 32K instruction cache and 8K data cache.

2.3 Memory

BL616CL memory includes: 224K OCRAM for CPU applications, 160K WRAM for WiFi wireless data transmission and reception, and 4K HBN RAM for storing low-power data in PDS/HBN mode. Additionally, it supports embedded PSRAM.

2.4 DMA Controller

The DMA (Direct Memory Access) controller has 8 dedicated channels for managing data transfers between peripherals and memory to enhance CPU/bus efficiency. DMA supports four transfer types: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral modes.

DMA also supports LLI (Linked List Item) functionality, where a linked list predefines multiple transfers, and the hardware automatically completes all transfers based on the size and address of each LLI.

Supported peripherals include UART, I2C, SPI, Audio (AUPWM and AUSOLO), GPIO, I2S, DBI, PEC, GPADC, and Timer.

2.5 Memory Map

Table 2.1: Memory address map

Module	Size	Start Address	
		Cache	Non-cache
OCRAM	224KB	0x60FC0000	0x20FC0000
WRAM	160KB	0x60FF8000	0x20FF8000

OCRAM and WRAM can be accessed via both the AHB and AXI buses. When the CPU accesses OCRAM at address 0x60FC0000, it goes through the internal cache and accesses OCRAM via the AXI bus. When the CPU accesses OCRAM at address 0x20FC0000, it does not go through the internal cache and accesses OCRAM directly via the AHB bus. When the CPU accesses WRAM at address 0x60FF8000, it goes through the internal cache and accesses WRAM via AXI to AHB.

Table 2.2: Memory Map

Module	Target	Start Address	Size	Description
FLASH	Flash	0x80000000	128MB	Application address space
PSRAM	pSRAM	0x88000000	128MB	pSRAM memory address space (optional, depending on the specific chip model)

Table 2.2: Memory Map(continued)

Module	Target	Start Address	Size	Description
RAM	HBN RAM	0x20010000	4KB	HBN RAM, mainly used for data storage in ultra-low power mode
	USB	0x20072000	4KB	USB High Speed OTG control register
	EMAC	0x20070000	4KB	EMAC control register
	SDIO Host	0x20060000	4KB	SDIO Host control register
	PEC	0x2005A000	4KB	Peripheral Expand Controller
	MJPEG	0x20059000	4KB	MJPEG image encoding control register
	DVP	0x20057000	4KB	DVP camera interface control register
	Efuse	0x20056000	1KB	Efuse storage control register
	AUPWM	0x20055000	4KB	AUPWM control register
	PSRAM_Ctrl	0x20052000	4KB	PSRAM control register
	HBN	0x2000F000	4KB	Hibernate register
	PDS	0x2000E000	4KB	Power-down sleep register
	SDIO	0x2000D000	4KB	SDIO device control register
	DMA	0x2000C000	4KB	DMA control register
	SF_Ctrl	0x2000B000	4KB	Serial Flash control register
	SPI1	0x2000AE00	256B	SPI1 control register
	UART2	0x2000AD00	256B	UART2 control register
	AUSOLO	0x2000AC00	256B	AUSOLO control register
	I2S	0x2000AB00	256B	I2S control register
	I2C1	0x2000A900	256B	I2C1 control register
	Display	0x2000A800	256B	Display control register
	TIMER	0x2000A500	256B	TIMER control register
	PWM	0x2000A400	256B	PWM control register
	I2C0	0x2000A300	256B	I2C0 control register
	SPI0	0x2000A200	256B	SPI0 control register
	UART1	0x2000A100	256B	UART1 control register
	UART0	0x2000A000	256B	UART0 control register
	TZ	0x20005000	4KB	TrustZone control register
	SEC_ENG	0x20004000	4KB	Security Engine control register
	GPADC	0x20002000	1KB	General ADC interface control register
	GLB	0x20000000	4KB	Global control register

2.6 Interrupt

The interrupt controller supports a total of 67 maskable interrupt sources triggered by UART /I2C /SPI /Timer /DMA /EMAC /WiFi /BLE, etc.

All I/O pins can be configured as external interrupt input modes, supporting synchronous high/low level triggering, synchronous rising/falling edge triggering, asynchronous high/low level triggering, asynchronous rising/falling edge triggering, and synchronous dual-edge triggering, totaling 9 triggering types.

2.7 Boot

BL616CL supports multiple boot options: UART, USB, SDU and Flash.

Table 2.3: Boot Mode

Boot Pin	Level	Description
GPIO36	1	Boot from UART(GPIO34/35)/USB(GPIO32/33)/SDU, mainly used for Flash programming or downloading programs to RAM for execution (wireless transparent transmission scenario)
	0	Boot application from Flash

2.8 Power

The Power Management Unit (PMU) manages power for the entire chip, which has 8 power domains: PD_AON/PD_AON_HBNRTC/PD_AON_HBNCORE/PD_CORE/PD_CORE_MISC/PD_USB/PD_CPU/PD_WB. The supported low power modes include Run, Idle, PDS, HBN and Power Off. In PDS and HBN modes, multiple wake-up sources can wake the system from low power mode.

2.9 Clock Architecture

Clock control unit generates clocks to the core MCU and the peripheral SOC devices.The root clock source can be XTAL, PLL or RC oscillator. Users can set the clock frequency of each peripheral or switch the clock of peripherals through appropriate configurations (e.g., sel, div, en, etc.) to meet low-power application requirements.

2.10 Peripheral

2.10.1 GPIO

BL616CL supports up to 37 (QFN48) or 29 (QFN40) or 21 (QFN32) GPIOs，which can be used as general-purpose input, output, and interrupt functions, and can also be reused for peripheral and analog functions:

- Each GPIO can be used for general input and output functions, with pull-up/pull-down/floating configurations available via software.
- Each GPIO supports interrupt functionality, with interrupts supporting synchronous high/low level triggering, synchronous rising/falling edge triggering, asynchronous high/low level triggering, asynchronous rising/falling edge triggering, and synchronous dual-edge triggering.
- Each GPIO can be set to high-impedance state for low-power mode.
- Each GPIO can control output state via Set/Clear registers.
- Supports custom logic 0/1 waveform output.
- Supports DMA.

2.10.2 DVP

DVP (Digital Video Port) is used for transmitting image data between the image sensor and the chip, with the following features:

- 8-bit parallel data width.
- Supports data formats such as YUV444/RGB888 (24-bit), YUV422/RGB565 (16-bit), YUV400 (8-bit) for input and output in the original format.
- Supports converting RGB888 input format to RGB565/RGBA8888 format output.
- Supports converting YUV422 input format to YUV420/400 format output.
- Configurable line/frame synchronization signal selection and polarity selection.
- Supports image rectangular cropping.
- Frame sampling function with a period of 1~32.
- Supports integrity detection of line/frame synchronization signals.
- Supports completion interrupts.

2.10.3 MJPEG Encoder

The MJPEG encoder is used to encode uncompressed image data streams, supporting the following features:

- Input data streams can be read directly from RAM or synchronized with DVP.
- Input images support YUV420SP, YUV400, YUV422SP, YUV422I color spaces.
- Supports enabling/disabling automatic copying of JPEG file headers.
- Two programmable quantization tables.
- Output data streams support double buffering.
- Only supports standard Huffman coding tables.
- Supports re-setting the original image data address after compressing a custom number of lines.
- Supported interrupts include: one frame compression complete, buffer full in double buffering mode.

2.10.4 DBI

The DBI (Display Bus Interface) module has 8-bit parallel data lines for driving screens with memory, featuring the following characteristics:

- Supports Type-B (8-bit), Type-C Option 1 (3-wire), and Type-C Option 3 (4-wire) modes.
- Supports RGB565/666/888 output formats.
- Supports QSPI mode, with CMD/ADDR/DATA configurable in 1-/4-wire modes.
- Supports RGB565/RGB888/RGBA8888/YUV444 input formats.
- Supports DMA functionality.

2.10.5 UART

The chip has three general-purpose asynchronous serial transceivers (UART0/1/2), featuring the following characteristics:

- Supports hardware CTS and RTS flow control.
- Supports LIN master/slave functionality.
- Configurable data bits, stop bits, and parity bits.
- Supports automatic baud rate detection for normal/fixed characters.

- The working clock can be selected as BCLK, XCLK, or 160MHz, with a maximum baud rate of 10Mbps.
- TX and RX have independent FIFO, with a FIFO depth of 32 bytes, supporting DMA functionality.
- Supports RTO timeout detection mechanism.
- Supports glitch filtering functionality.
- Supports RS-485 mode.

2.10.6 SPI

The chip has two built-in SPI interfaces, configurable as master or slave mode, with the SPI module clock being XCLK or 160MHz, featuring the following characteristics:

- In master mode, the maximum clock frequency is 80 MHz.
- In slave mode, the maximum clock frequency allowed by the master is 80 MHz.
- The bit width of each frame can be configured as 8 bits/16 bits/24 bits/32 bits.
- Adaptive FIFO depth variation characteristics to suit high-performance application scenarios.

2.10.7 I2C

The chip has two built-in I2C interfaces, featuring the following characteristics:

- Supports multi-master mode and arbitration functionality.
- Supports a maximum packet length of 1024 bytes.
- Supports timeout functionality.
- The working clock can be selected as BCLK or XCLK.
- Supports Standard-mode (up to 100KHz) and Fast-mode (up to 400KHz), with a maximum speed of 1.8MHz (depending on the external pull-up resistor).
- Supports 7-bit and 10-bit device addresses.
- Supports 0~16 bytes of register addresses.
- I2C has independent transmit/receive FIFO, with a FIFO depth of 2, width of 32 bits.
- Supports DMA functionality.

2.10.8 EMAC

The EMAC module is a 10/100Mbps Ethernet MAC (Ethernet Media Access Controller) compatible with IEEE 802.3, featuring the following characteristics:

- Compatible with MAC layer functions defined by IEEE 802.3.
- Supports PHY with RMII interface defined by IEEE 802.3.
- Interacts with PHY via MDIO interface.
- Supports 100Mbps and 10Mbps Ethernet.
- Supports half-duplex and full-duplex modes.
- In full-duplex mode, supports automatic flow control and generates control frames.
- In half-duplex mode, supports collision detection and retransmission.
- Supports CRC generation and verification.
- Generates and removes data frame preambles.
- Automatically extends short data frames during transmission.
- Detects overly long or short data frames (length limits).
- Can transmit long data frames (> standard Ethernet frame length).
- Automatically discards packets exceeding retransmission limits or with insufficient frame gaps.
- Broadcast packet filtering.
- Internal RAM for saving up to 128 BD (Buffer Descriptor).
- During transmission, supports splitting a data packet across multiple consecutive BDs.
- Various event flags for sending/receiving.
- Generates corresponding interrupts when events occur.

2.10.9 I2S

The chip has a built-in I2S interface, featuring the following characteristics:

- Supports master and slave modes.
- Supports Left-justified/Right-justified/DSP data formats, with data width configurable as 8/16/24/32 bits.

- The working clock is WIFIPLL 320MHz.
- In addition to mono/stereo modes, supports four-channel and six-channel modes.
- Supports playing mono audio copied to stereo mode.
- Supports dynamic mute switching functionality.
- I2S has independent transmit/receive FIFO, with a FIFO depth of 16 words.
- Supports DMA functionality.

2.10.10 TIMER

The chip has two 32-bit general-purpose timers and two watchdog timer, featuring the following characteristics:

- The clock source for general-purpose timers can be selected as FCLK/32K/XTAL/GPIO, while the clock source for the watchdog timer can be selected as FCLK/32K/XTAL/GPIO.
- Each counter has an 8-bit prescaler.
- Each group of general-purpose timers includes three comparison registers, supporting comparison interrupts, with counting modes supporting FreeRun mode and PreLoad mode.
- The 16-bit watchdog timer supports two overflow modes: interrupt or reset.
- Both general-purpose timers support initiating DMA transfer requests.
- General-purpose timer 0 supports external input capture.

2.10.11 GPADC

The chip has a built-in GPADC, featuring the following characteristics:

- Configurable 16-bit, 14-bit, and 12-bit resolutions.
- Maximum sampling rate of 2Msps.
- Supports differential and single-ended sampling.
- Supports single conversion mode, continuous conversion mode, single scan conversion mode, and continuous scan conversion mode.
- Supports injecting other channels during the conversion process of regular channels.
- Built-in PGA, with gain adjustable from 1 to 32 times, with each step being 6dB.

- Both regular and injected channels support independent FIFO, with a FIFO depth of 32, and both support DMA transfer.
- Supports FIFO_RDY interrupts, with customizable FIFO_RDY thresholds.
- Supports sampling of 4 internal channels and 12 external channels, with internal channels including VBAT/2, TSEN, etc.
- Built-in temperature sensor implements a temperature conversion function based on a temperature-dependent voltage.

2.10.12 PWM

The chip has a set of PWM signals, with each set containing 4 channels of PWM signal output, and each channel can be set to 2 complementary PWM paths, featuring the following characteristics:

- Three clock sources (BCLK/XCLK/32K) are available, paired with a 16-bit clock prescaler.
- All 4 channels of PWM signals share the same PWM period.
- Each PWM channel has dual threshold value settings, allowing different duty cycles and phases, increasing pulse elasticity.
- Maximum frequency of 40 MHz with a duty cycle of 50%, minimum frequency less than 1Hz and an adjustable duty cycle
- Each PWM channel has independent dead time settings.
- Each PWM output pin can be set to different active levels.
- Each PWM has an independent connection switch to choose whether to connect to the internal counter, with a default output level set when not connected.
- Brake signals can set the PWM output level to a pre-defined state.
- Up to 11 trigger sources can be used to trigger GPADC conversions.
- Supports various interrupt types: counter overflow interrupt, threshold comparison interrupt, and cycle count interrupt.

2.10.13 AUSOLO

The AUSOLO only supports PDM interface (supports 1 channel DMIC), featuring the following characteristics:

- Adjustable high-pass filter and digital volume control.
- Input signal multiplexed with GPIO.
- 32-bit width receive FIFO, depth of 8.
- Supports DMA transfer mode.

2.10.14 AUPWM

- Integrates 1 AUPWM module that converts audio data into sigma-delta modulated PWM signals output through GPIO, featuring the following characteristics:
  - Sampling rate: 8k~48k
  - Signal-to-noise ratio (A-W): 95dB @ 48K sampling rate
  - Harmonic distortion + noise: -80dB @ 48K sampling rate
- Adjustable digital volume control.
- Supports differential complementary output.
- Output signal multiplexed with GPIO.
- 32-bit width transmit FIFO, depth of 16.
- Supports DMA transfer mode.

2.10.15 PEC

The Peripheral Expand Controller is used to expand peripherals, with expandable peripherals including but not limited to UART, I2C, SPI, GPIO, JTAG, DPI, DBI, PWM, IR,etc., featuring the following characteristics:

- 2 independent state machines for expanding different peripherals.
- 32*32bits sending FIFO and 16*32bits receiving FIFO for state machine 0，8*32bits sending FIFO and 8*32bits receiving FIFO for state machine 0.
- Instruction space for state machine 0 is 128, and for state machine 1 is 64.
- Supports 9 types of control instructions and 26 types of computational instructions.

- Flexible GPIO mapping.
- 8 internal registers (including ISR, OSR, and 6 general-purpose registers).
- Supports DMA transfer mode.
- Input pins support debouncing functionality.

2.10.16 SDIO3.0 Host

SDH is the SD bus interface host controller, used to control and manage SD storage cards, SDIO cards, etc., providing data storage and expansion functionality. It has the following features:

- Complies with SD Host Controller Standard Specification Version 3.0.
- Complies with SD 3.0 Physical Layer Specification Version 3.01.
- Complies with SDIO Specification Version 3.0.
- Supports LS/DS/HS rates.
- Supports ADMA1, ADMA2.

2.10.17 SDIO Device

The timing diagram for the SDIO Device is as follows:

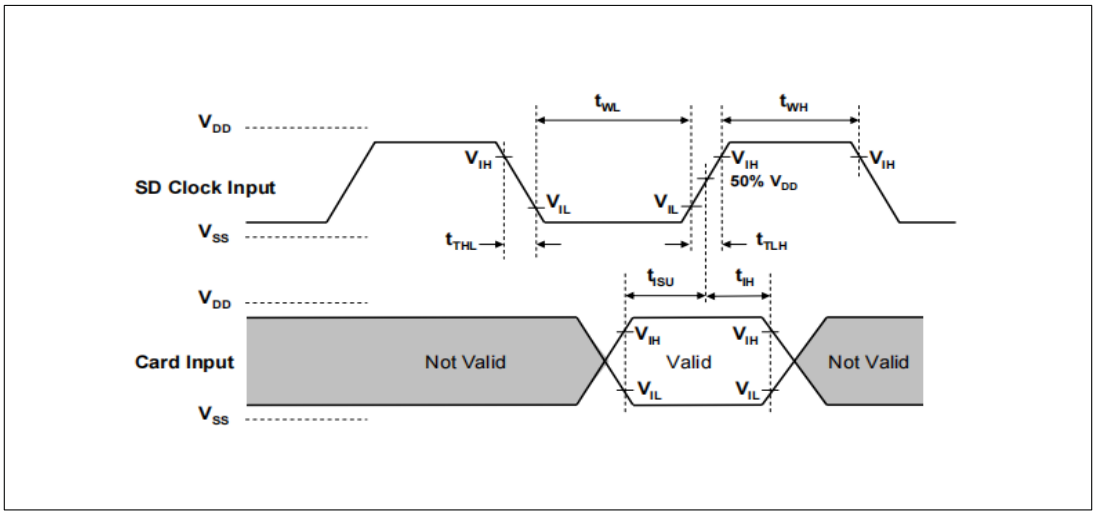


Fig. 2.2: Card Input Timing Diagram

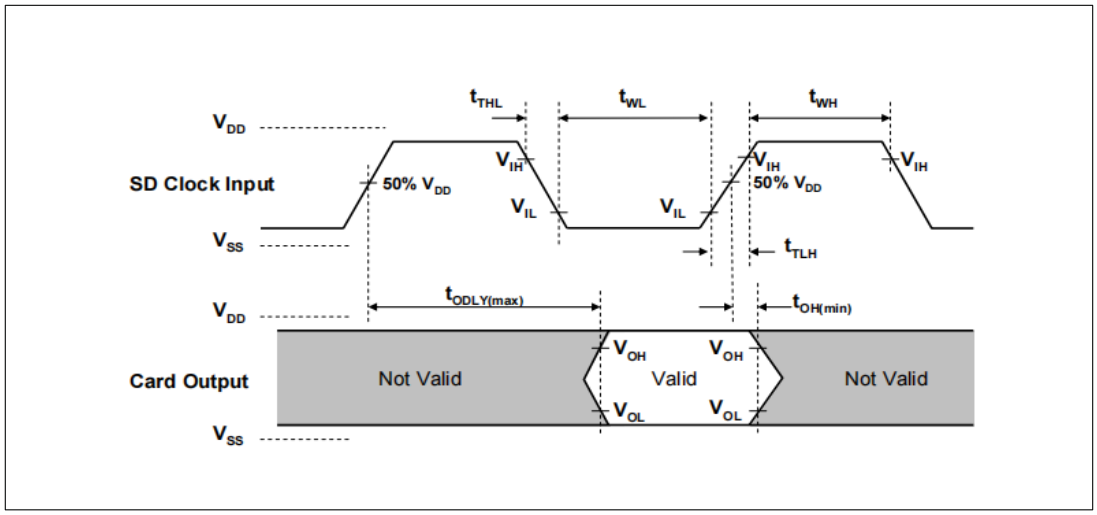


Fig. 2.3: Card Output Timing Diagram

Table 2.4: Timing Diagram Parameter Description

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Clock CLK (All values are referred to min (VIH) and max (VIL))						
f_{PP}	Clock frequency Data Transfer Mode	C_{CARD}≤ 10 pF (1 card)	0		50	MHz
t_{WL}	Clock low time	C_{CARD}≤ 10 pF (1 card)	7			ns
t_{WH}	Clock high time	C_{CARD}≤ 10 pF (1 card)	7			ns
t_{TLH}	Clock rise time	C_{CARD}≤ 10 pF (1 card)			3	ns
t_{THL}	Clock fall time	C_{CARD}≤ 10 pF (1 card)			3	ns
Inputs CMD, DAT (referenced to CLK)						
t_{ISU}	Input set-up time	C_{CARD}≤ 10 pF (1 card)	6			ns
t_{IH}	Input hold time	C_{CARD}≤ 10 pF (1 card)	2			ns
Outputs CMD, DAT (referenced to CLK)						
t_{ODLY}	Output Delay time during Data Transfer Mode	C_L≤ 40 pF (1 card)			14	ns
t_{OH}	Output Hold time	C_L≥ 15 pF (1 card)	2.5			ns

Table 2.4: Timing Diagram Parameter Description(continued)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
C_L	Total System capacitance for each line [1]	1 card			40	pF

[1] In order to satisfy stringent timing, host shall drive only one card.

2.10.18 USB

USB (Universal Serial Bus) is a universal bus standard used to specify the connection and communication between computers and external devices. The chip supports USB2.0 (HighSpeed + FullSpeed) and can function as a host controller or device controller. As a host controller, it includes a USB host controller that supports low-speed, full-speed, and high-speed devices. Without software intervention, the host controller can autonomously handle transaction-based data structures to reduce CPU load and automatically send and receive data on the USB bus. When functioning as a device controller, each endpoint, except endpoint 0, supports the transmission types specified by the USB standard to meet various application scenarios.

General features include:

- Compliant with USB2.0 standard.
- Built-in high-speed PHY.
- Can be configured via software to operate in HOST mode or DEVICE mode.

HOST mode features are as follows:

- Compliant with EHCI 1.0 standard (does not support FSTN and SITD).
- Supports enumeration of high-speed, full-speed, and low-speed devices.

DEVICE mode features are as follows:

- Supports high-speed and full-speed devices.
- 1 bi-directional control endpoint 0.
- 8 bi-directional endpoints (supporting IN/OUT), configurable for bulk transfer, interrupt transfer, and synchronous transfer.
- Built-in dedicated DMA (DMA, VDMA), does not support direct FIFO reading.
- Shares 8 buffers of 512 bytes, which can be flexibly configured into single-buffer, double-buffer, or triple-buffer modes.
- Supports suspend, resume, and remote wake-up functionalities.

- Supports soft disconnection functionality.

2.10.19 Flash Controller

The Flash controller supports XIP (Execute In Place), allowing code to be executed directly from Flash, thereby reducing RAM usage. It features the following characteristics:

- Clock source can be selected from Wifipll 80M/96M/120M/160M, XTAL, or BCLK
- Flash frequency can reach up to 80 MHz
- Compatible with SPI, Dual SPI, and Quad SPI interfaces
- Support Flash erase/read/write operations
- Support hardware XIP decryption, with AES CTR/XTS modes
- Support 24-bit and 32-bit address modes for Flash
- Support both internal and external Flash memory

2.10.20 Secure Boot

The chip supports the Secure Boot feature, which verifies the Bootloader and application firmware during the startup process to ensure their integrity and authenticity, effectively preventing the execution of unauthorized code. It features the following characteristics:

- Signature Verification: Support signature verification based on SECP256R1/SECP384R1.
- Firmware Encryption: Support AES CTR/XTS encryption algorithms.
- Anti-Rollback Protection: Prevent downgrade attacks, ensuring the device runs the latest or specified firmware version.

2.10.21 SEC_ENG

The SEC ENG module incorporates a variety of cryptographic operation units, including AES, SHA, CRC, GMAC, PKA, and TRNG.

- AES
  - Support 128-bit, 192-bit and 256-bit key lengths
  - Support encryption and decryption of multiple link modes (ECB/CBC/CTR/XTS)
  - The key is stored in eFuse with read and write protection

  - Support AES LINK function

- SHA
  - Support SHA1/SHA224/SHA256/SHA384/SHA512
  - Support SHA LINK function
- TRNG
  - Generate a 256-bit random number in a single operation
  - Physical random number generator
- CRC
  - Support CRC-16 and CRC-32

2.10.22 TOUCH

The chip integrates one touch controller, capable of scanning up to 8 channels in self-scan mode and up to 16 channels in mutual-scan mode. It features the following characteristics:

- Configurable channel scan time
- Supports touch detection and touch release detection
- Scan results support filtering to reduce the impact of noise signals
- Supports low-power scan mode
- Supports frequency-hopping mode to reduce the impact of co-channel interference
- Touch detection supports configurable touch duration
- Supports both self-scan and mutual-scan modes

3 Pin Definition

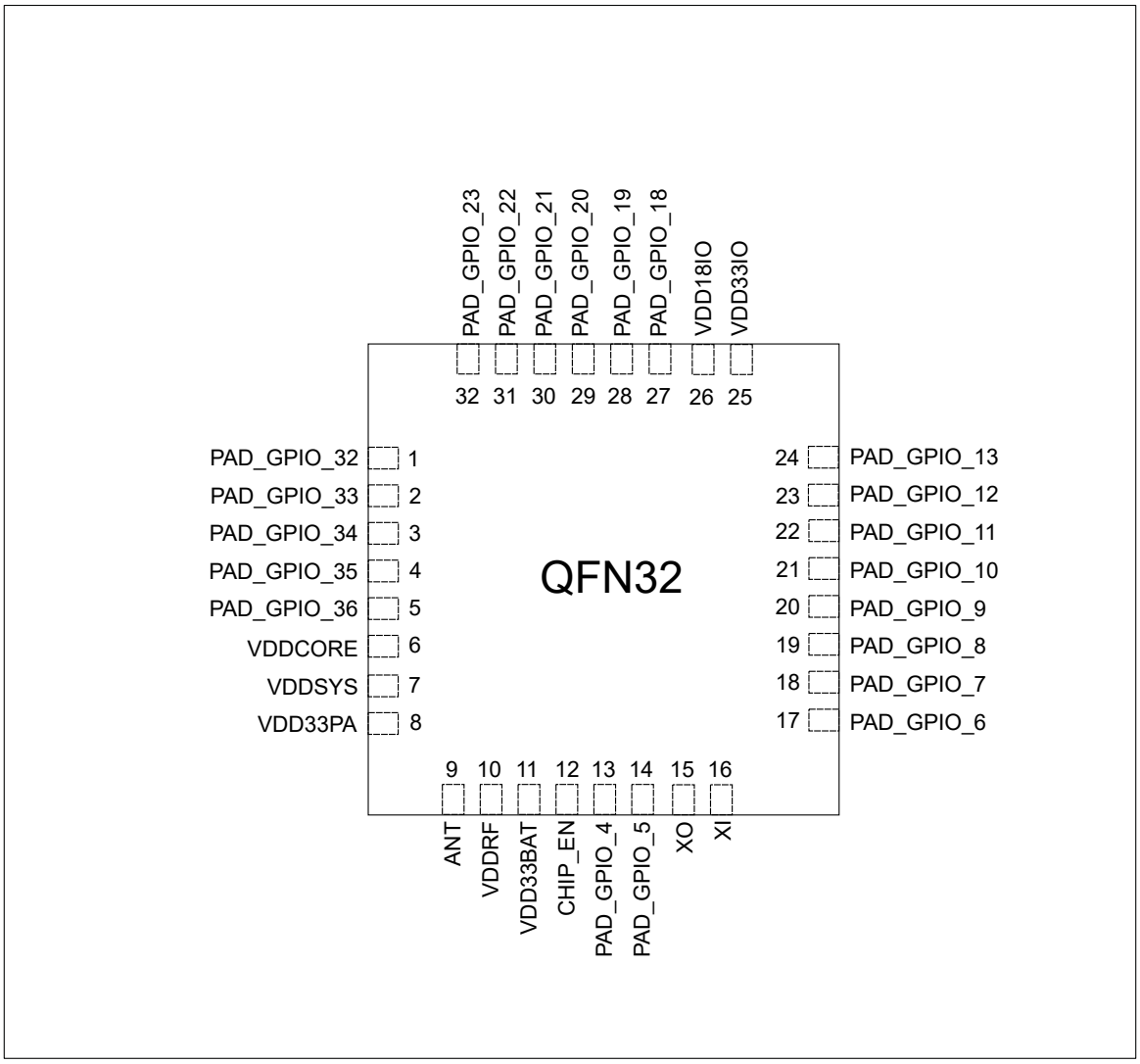


Fig. 3.1: QFN32 pin layout

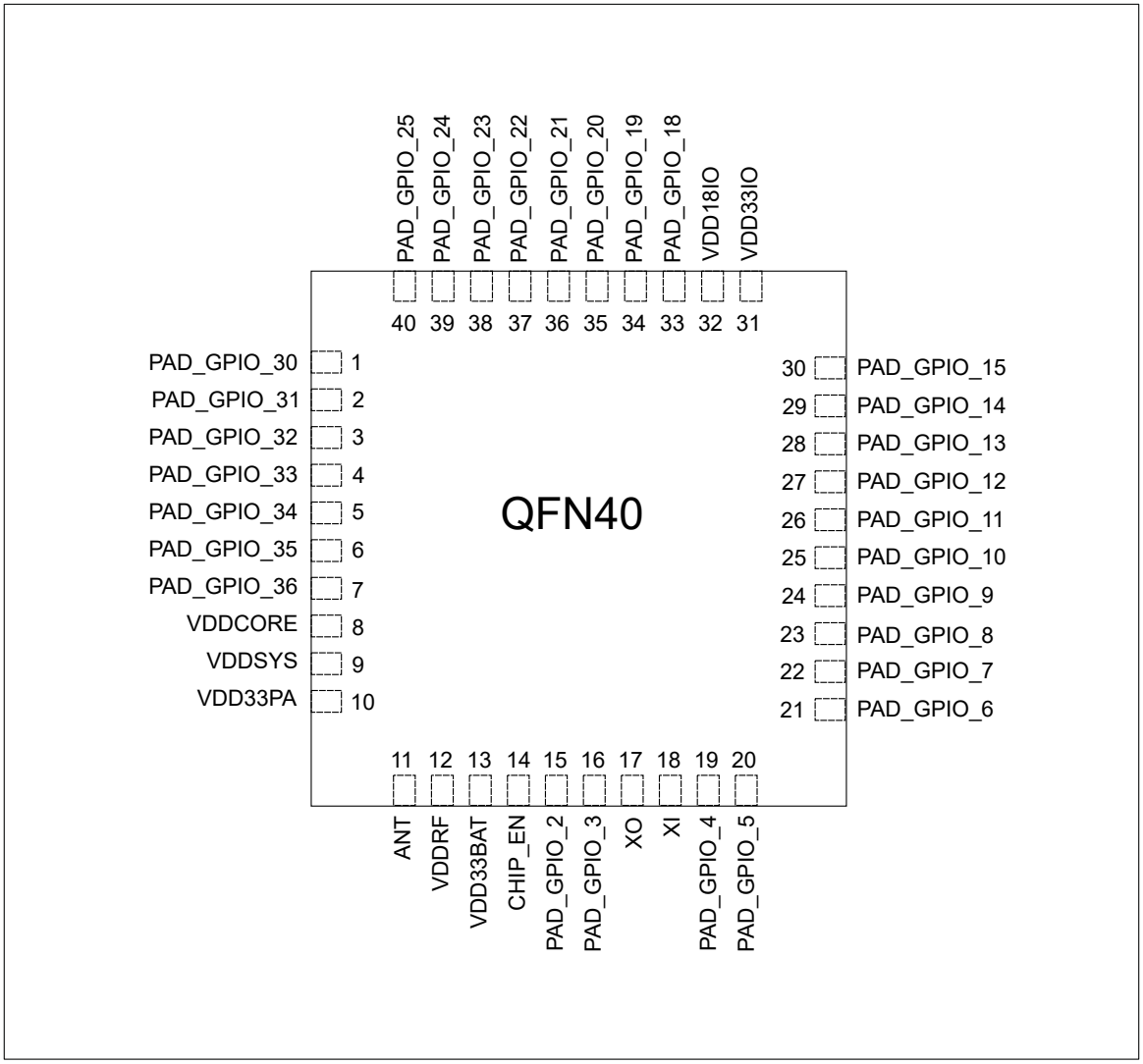


Fig. 3.2: QFN40 pin layout

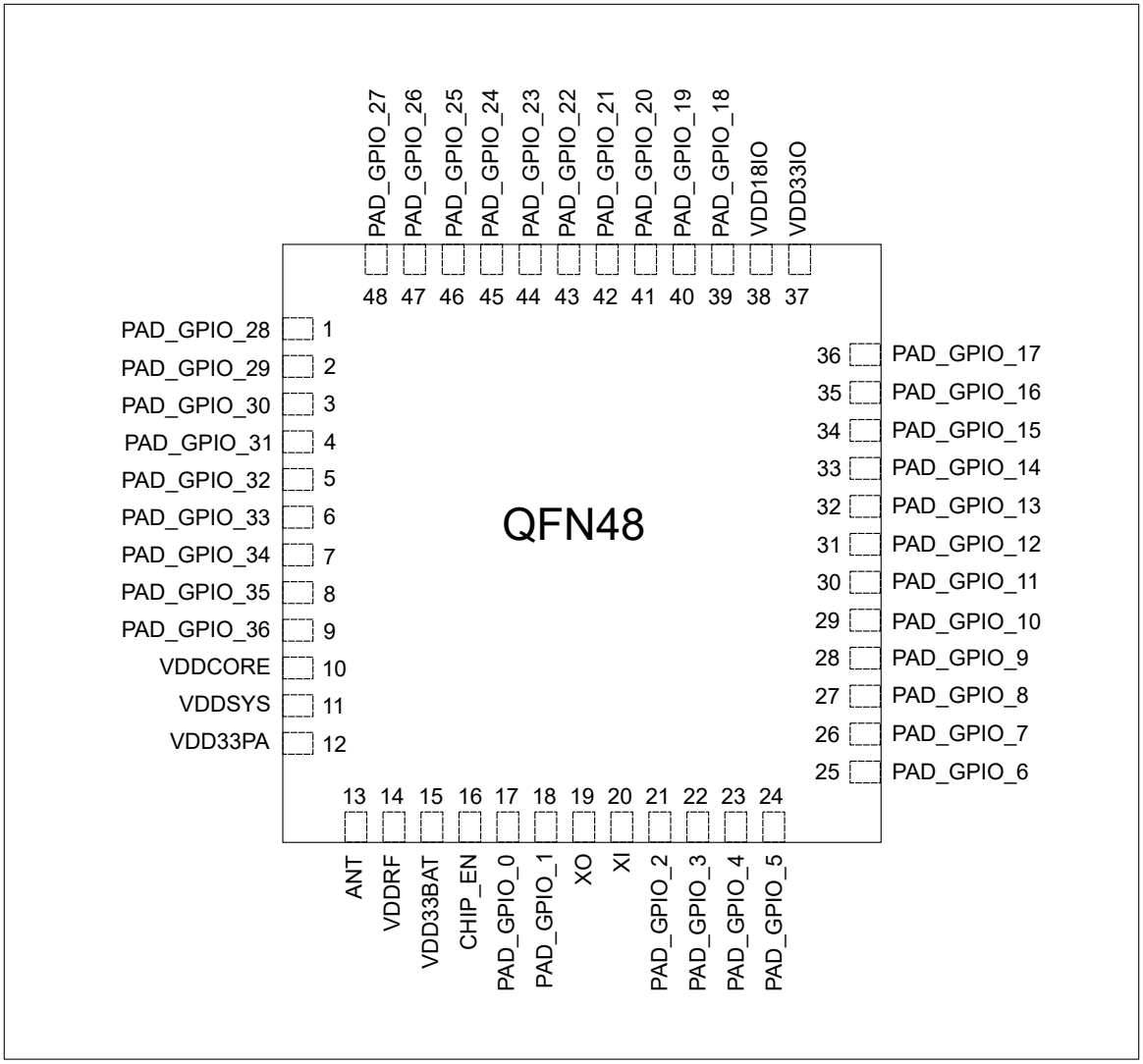


Fig. 3.3: QFN48 pin layout

Table 3.1: Pin definition

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	-	1		DI/DO	PAD_GPIO_28	0	-	-	-
						1	-	SPI0_SS	SPI 0 Slave Select
						2	-	SF3_D1	NOR FALSH controller signal3 Data 1
						3	-	I2S_BCLK	I2S Bit Clock
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG4 [1]	-
						8	-	RMII_REF_CLK	RMII Reference Clock
						9	-	CAM_DAT2	Camera Data 2
						10	-	-	-
						11	-	SWGPIO[28]	Software GPIO 28
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
							reg_pwm1_io_sel=1	PWM0_CH2P	PWM0 Channel 2 Positive
						20	-	SPI1_SS	SPI 1 Slave Select
						22	-	DBI_TypeB_DB4	Display Bus Interface Type B Data Bit 4
						23	-	DBI_TypeC_SDA	Display Bus Interface Type C Serial Data
						24	-	DISP_QSPI_SDA2	Display Quad SPI Serial Data 2
						25	-	-	-
						26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
						27	-	PEC_28	PEC_28
						31	-	chip_clk_out[0]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	-	2		DI/DO	PAD_GPIO_29	0	-	-	-
						1	-	SPI0_SCLK	SPI 0 Serial Clock
						2	-	SF3_CS	NOR FALSH controller signal3 Chip Select
						3	-	I2S_FS	I2S Frame Sync
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG5	-
						8	-	RMII_RXD[1]	RMII Receive Data[1]
						9	-	CAM_DAT3	Camera Data 3
						10	-	-	-
						11	-	SWGPIO[29]	Software GPIO 29
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
							reg_pwm1_io_sel=1	PWM0_CH2N	PWM0 Channel 2 Negative
						20	-	SPI1_SCLK	SPI 1 Serial Clock
						22	-	DBI_TypeB_DB5	Display Bus Interface Type B Data Bit 5
						23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control
						24	-	DISP_QSPI_SDA3	Display Quad SPI Serial Data 3
						25	-	-	-
						26	-	M0_JTAG_TCK	M0 JTAG Test Clock
						27	-	PEC_29	PEC_29
						31	-	chip_clk_out[1]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	1	3		DI/DO	PAD_GPIO_30	0	-	-	-
						1	-	SPI0_MISO [2]	SPI 0 Master Input, Slave Output
						2	-	-	-
						3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG6	-
						8	-	RMII_RXD[0]	RMII Receive Data[0]
						9	-	CAM_DAT6	Camera Data 6
						10	-	-	-
						11	-	SWGPIO[30]	Software GPIO 30
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
							reg_pwm1_io_sel=1	PWM0_CH3P	PWM0 Channel 3 Positive
						20	-	SPI1_MISO	SPI 1 Master Input, Slave Output
						22	-	DBI_TypeB_DB6	Display Bus Interface Type B Data Bit 6
						23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock
						24	-	-	-
						25	-	AUPWM_P	AUPWM_P
						26	-	M0_JTAG_TDO	M0 JTAG Test Data Out
						27	-	PEC_30	PEC_30
						31	-	chip_clk_out[2]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	2	4		DI/DO	PAD_GPIO_31	0	-	-	-
						1	-	SPI0_MOSI	SPI 0 Master Output, Slave Input
						2	-	-	-
						3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG7	-
						8	-	RMII_RX_DV	RMII Receive Data Valid
						9	-	CAM_DAT7	Camera Data 7
						10	-	-	-
						11	-	SWGPIO[31]	Software GPIO 31
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
							reg_pwm1_io_sel=1	PWM0_CH3N	PWM0 Channel 3 Negative
						20	-	SPI1_MOSI	SPI 1 Master Output, Slave Input
						22	-	DBI_TypeB_DB7	Display Bus Interface Type B Data Bit 7
						23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select
						24	-	-	-
						25	-	AUPWM_N	AUPWM_N
						26	-	M0_JTAG_TDI	M0 JTAG Test Data Input
						27	-	PEC_31	PEC_31
						31	-	chip_clk_out[3]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
1	3	5		DI/DO	PAD_GPIO_32	0	-	-	-
						1	-	SPI0_SS	SPI 0 Slave Select
						2	-	-	-
						3	-	I2S_BCLK	I2S Bit Clock
						4	-	pdm_clk	PDM Clock Line
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG8	-
						8	-	-	-
						9	-	-	-
						10	-	USB_DP/ADC_CH10	USB_DP/ADC Channel 10
						11	-	SWGPIO[32]	Software GPIO 32
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
							reg_pwm1_io_sel=1	PWM0_CH0P	PWM0 Channel 0 Positive
						20	-	SPI1_SS	SPI 1 Slave Select
						22	-	-	-
						23	-	DBI_TypeC_SDA	Display Bus Interface Type C Serial Data
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
						27	-	PEC_32	PEC_32
						31	-	chip_clk_out[0]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
2	4	6		DI/DO	PAD_GPIO_33	0	-	-	-
						1	-	SPI0_SCLK	SPI 0 Serial Clock
						2	-	-	-
						3	-	I2S_FS	I2S Frame Sync
						4	-	pdm_in	PDM Data Line
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG9	-
						8	-	-	-
						9	-	-	-
						10	-	USB_DM/ADC_CH11	USB_DM/ADC Channel 11
						11	-	SWGPIO[33]	Software GPIO 33
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
							reg_pwm1_io_sel=1	PWM0_CH0N	PWM0 Channel 0 Negative
						20	-	SPI1_SCLK	SPI 1 Serial Clock
						22	-	-	-
						23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TCK	M0 JTAG Test Clock
						27	-	PEC_33	PEC_33
						31	-	chip_clk_out[1]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
3	5	7		DI/DO	PAD_GPIO_34	0	-	-	-
						1	-	SPI0_MISO	SPI 0 Master Input, Slave Output
						2	-	-	-
						3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG10	-
						8	-	-	-
						9	-	-	-
						10	-	-	-
						11	-	SWGPIO[34]	Software GPIO 34
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
							reg_pwm1_io_sel=1	PWM0_CH1P	PWM0 Channel 1 Positive
						20	-	SPI1_MISO	SPI 1 Master Input, Slave Output
						22	-	-	-
						23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TDO	M0 JTAG Test Data Out
						27	-	PEC_34	PEC_34
						31	-	chip_clk_out[2]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
4	6	8		DI/DO	PAD_GPIO_35	0	-	-	-
						1	-	SPI0_MOSI	SPI 0 Master Output, Slave Input
						2	-	-	-
						3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG11	-
						8	-	-	-
						9	-	-	-
						10	-	-	-
						11	-	SWGPIO[35]	Software GPIO 35
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
							reg_pwm1_io_sel=1	PWM0_CH1N	PWM0 Channel 1 Negative
						20	-	SPI1_MOSI	SPI 1 Master Output, Slave Input
						22	-	-	-
						23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TDI	M0 JTAG Test Data Input
						27	-	PEC_35	PEC_35
						31	-	chip_clk_out[3]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
5	7	9		DI/DO	PAD_GPIO_36	0	-	-	-
						1	-	SPI0_SS	SPI 0 Slave Select
						2	-	-	-
						3	-	I2S_BCLK	I2S Bit Clock
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG0	-
						8	-	-	-
						9	-	-	-
						10	-	-	-
						11	-	SWGPIO[36]	Software GPIO 36
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
							reg_pwm1_io_sel=1	PWM0_CH2P	PWM0 Channel 2 Positive
						20	-	SPI1_SS	SPI 1 Slave Select
						22	-	DBI_TypeB_DCn	Display Bus Interface Type B Data /Command Control
						23	-	-	-
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
						27	-	PEC_36	PEC_36
						31	-	chip_clk_out[0]	Internal Clock Output of the Chip
6	8	10		Power,Input	VDDCORE	-	-	-	-
7	9	11		Power,Input	VDDSYS	-	-	-	-
8	10	12		Power,Input	VDD33PA	-	-	-	-
9	11	13		Analog	ANT	-	-	-	-
10	12	14		Power,Input	VDDRF	-	-	-	-
11	13	15		Power,Input	VDD33BAT	-	-	-	-
12	14	16		Analog	CHIP_EN	-	-	-	-
15	17	19		Clock	XO	-	-	-	-
16	18	20		Clock	XI	-	-	-	-

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	-	17		DI/DO	PAD_GPIO_0	0	-	-	-
						1	-	SPI0_SS	SPI 0 Slave Select
						2	-	-	-
						3	-	I2S_BCLK	I2S Bit Clock
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG0	-
						8	-	-	-
						9	-	-	-
						10	-	ADC_CH0	ADC Channel 0
						11	-	SWGPIO[0]	Software GPIO 0
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
							reg_pwm1_io_sel=1	PWM0_CH0P	PWM0 Channel 0 Positive
						20	-	SPI1_SS	SPI 1 Slave Select
						22	-	DBI_TypeB_CSn	Display Bus Interface Type B Chip Select
						23	-	DBI_TypeC_SDA	Display Bus Interface Type C Serial Data
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
						27	-	PEC_0	PEC_0
						31	-	chip_clk_out[0]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	-	18		DI/DO	PAD_GPIO_1	0	-	-	-
						1	-	SPI0_SCLK	SPI 0 Serial Clock
						2	-	-	-
						3	-	I2S_FS	I2S Frame Sync
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG1	-
						8	-	-	-
						9	-	-	-
						10	-	ADC_CH1	ADC Channel 1
						11	-	SWGPIO[1]	Software GPIO 1
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
							reg_pwm1_io_sel=1	PWM0_CH0N	PWM0 Channel 0 Negative
						20	-	SPI1_SCLK	SPI 1 Serial Clock
						22	-	DBI_TypeB_RDn	Display Bus Interface Type B Read Control
						23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TCK	M0 JTAG Test Clock
						27	-	PEC_1	PEC_1
						31	-	chip_clk_out[1]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	15	21		DI/DO	PAD_GPIO_2	0	-	-	-
						1	-	SPI0_MISO	SPI 0 Master Input, Slave Output
						2	-	-	-
						3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG2	-
						8	-	-	-
						9	-	-	-
						10	-	ADC_CH2	ADC Channel 2
						11	-	SWGPIO[2]	Software GPIO 2
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
							reg_pwm1_io_sel=1	PWM0_CH1P	PWM0 Channel 1 Positive
						20	-	SPI1_MISO	SPI 1 Master Input, Slave Output
						22	-	DBI_TypeB_WRn	Display Bus Interface Type B Write Control
						23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TDO	M0 JTAG Test Data Out
						27	-	PEC_2	PEC_2
						31	-	chip_clk_out[2]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	16	22		DI/DO	PAD_GPIO_3	0	-	-	-
						1	-	SPI0_MOSI	SPI 0 Master Output, Slave Input
						2	-	-	-
						3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG3	-
						8	-	-	-
						9	-	-	-
						10	-	ADC_CH3	ADC Channel 3
						11	-	SWGPIO[3]	Software GPIO 3
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
							reg_pwm1_io_sel=1	PWM0_CH1N	PWM0 Channel 1 Negative
						20	-	SPI1_MOSI	SPI 1 Master Output, Slave Input
						22	-	DBI_TypeB_DCn	Display Bus Interface Type B Data /Command Control
						23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TDI	M0 JTAG Test Data Input
						27	-	PEC_3	PEC_3
						31	-	chip_clk_out[3]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
13	19	23		DI/DO	PAD_GPIO_4	0	-	-	-
						1	-	SPI0_SS	SPI 0 Slave Select
						2	-	-	-
						3	-	I2S_BCLK	I2S Bit Clock
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG4	-
						8	-	-	-
						9	-	-	-
						10	-	ADC_CH4	ADC Channel 4
						11	-	SWGPIO[4]	Software GPIO 4
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
							reg_pwm1_io_sel=1	PWM0_CH2P	PWM0 Channel 2 Positive
						20	-	SPI1_SS	SPI 1 Slave Select
						22	-	-	-
						23	-	DBI_TypeC_SDA	Display Bus Interface Type C Serial Data
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
						27	-	PEC_4	PEC_4
						31	-	chip_clk_out[0]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
14	20	24		DI/DO	PAD_GPIO_5	0	-	-	-
						1	-	SPI0_SCLK	SPI 0 Serial Clock
						2	-	-	-
						3	-	I2S_FS	I2S Frame Sync
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG5	-
						8	-	-	-
						9	-	-	-
						10	-	ADC_CH5	ADC Channel 5
						11	-	SWGPIO[5]	Software GPIO 5
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
							reg_pwm1_io_sel=1	PWM0_CH2N	PWM0 Channel 2 Negative
						20	-	SPI1_SCLK	SPI 1 Serial Clock
						22	-	-	-
						23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control
						24	-	-	-
						25	-	-	-
						26	-	M0_JTAG_TCK	M0 JTAG Test Clock
						27	-	PEC_5	PEC_5
						31	-	chip_clk_out[1]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
17	21	25		DI/DO	PAD_GPIO_6	0	-	SDH_DAT2	SD Host Data 2
						1	-	SPI0_MISO	SPI 0 Master Input, Slave Output
						2	-	SF2_CS [3]	NOR FALSH controller signal2 Chip Select
						3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG6	-
						8	-	-	-
						9	-	-	-
						10	-	ADC_CH6	ADC Channel 6
						11	-	SWGPIO[6]	Software GPIO 6
						12	-	SDIO_DAT2	SDIO_DAT2
						16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
							reg_pwm1_io_sel=1	PWM0_CH3P	PWM0 Channel 3 Positive
						20	-	SPI1_MISO	SPI 1 Master Input, Slave Output
						22	-	-	-
						23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock
						24	-	DISP_QSPI_SCL	Display Quad SPI Serial Clock
						25	-	-	-
						26	-	M0_JTAG_TDO	M0 JTAG Test Data Out
						27	-	PEC_6	PEC_6
						31	-	chip_clk_out[2]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
18	22	26		DI/DO	PAD_GPIO_7	0	-	SDH_DAT3	SD Host Data 3
						1	-	SPI0_MOSI	SPI 0 Master Output, Slave Input
						2	-	SF2_D1	NOR FALSH controller signal2 Data 1
						3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG7	-
						8	-	-	-
						9	-	-	-
						10	-	ADC_CH7	ADC Channel 7
						11	-	SWGPIO[7]	Software GPIO 7
						12	-	SDIO_DAT3	SDIO_DAT3
						16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
							reg_pwm1_io_sel=1	PWM0_CH3N	PWM0 Channel 3 Negative
						20	-	SPI1_MOSI	SPI 1 Master Output, Slave Input
						22	-	-	-
						23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select
						24	-	DISP_QSPI_CSn	Display Quad SPI Chip Select
						25	-	-	-
						26	-	M0_JTAG_TDI	M0 JTAG Test Data Input
						27	-	PEC_7	PEC_7
						31	-	chip_clk_out[3]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
19	23	27		DI/DO	PAD_GPIO_8	0	-	SDH_CMD	SD Host Command
						1	-	SPI0_SS	SPI 0 Slave Select
						2	-	SF2_D2	NOR FALSH controller signal2 Data 2
						3	-	I2S_BCLK	I2S Bit Clock
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG8	-
						8	-	-	-
						9	-	-	-
						10	-	-	-
						11	-	SWGPIO[8]	Software GPIO 8
						12	-	SDIO_CMD	SDIO_CMD
						16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
							reg_pwm1_io_sel=1	PWM0_CH0P	PWM0 Channel 0 Positive
						20	-	SPI1_SS	SPI 1 Slave Select
						22	-	-	-
						23	-	DBI_TypeC_SDA	Display Bus Interface Type C Serial Data
						24	-	DISP_QSPI_SDA0	Display Quad SPI Serial Data 0
						25	-	-	-
						26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
						27	-	PEC_8	PEC_8
						31	-	chip_clk_out[0]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
20	24	28		DI/DO	PAD_GPIO_9	0	-	SDH_CLK	SD Host Clock
						1	-	SPI0_SCLK	SPI 0 Serial Clock
						2	-	SF2_D0	NOR FALSH controller signal2 Data 0
						3	-	I2S_FS	I2S Frame Sync
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG9	-
						8	-	-	-
						9	-	-	-
						10	-	-	-
						11	-	SWGPIO[9]	Software GPIO 9
						12	-	SDIO_CLK	SDIO_CLK
						16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
							reg_pwm1_io_sel=1	PWM0_CH0N	PWM0 Channel 0 Negative
						20	-	SPI1_SCLK	SPI 1 Serial Clock
						22	-	-	-
						23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control
						24	-	DISP_QSPI_SDA1	Display Quad SPI Serial Data 1
						25	-	-	-
						26	-	M0_JTAG_TCK	M0 JTAG Test Clock
						27	-	PEC_9	PEC_9
						31	-	chip_clk_out[1]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
21	25	29		DI/DO	PAD_GPIO_10	0	-	SDH_DAT0	SD Host Data 0
						1	-	SPI0_MISO	SPI 0 Master Input, Slave Output
						2	-	SF2_CLK	NOR FALSH controller signal2 Clock
						3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG10	-
						8	-	-	-
						9	-	-	-
						10	-	-	-
						11	-	SWGPIO[10]	Software GPIO 10
						12	-	SDIO_DAT0	SDIO_DAT0
						16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
							reg_pwm1_io_sel=1	PWM0_CH1P	PWM0 Channel 1 Positive
						20	-	SPI1_MISO	SPI 1 Master Input, Slave Output
						22	-	-	-
						23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock
						24	-	DISP_QSPI_SDA2	Display Quad SPI Serial Data 2
						25	-	-	-
						26	-	M0_JTAG_TDO	M0 JTAG Test Data Out
						27	-	PEC_10	PEC_10
						31	-	chip_clk_out[2]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
22	26	30		DI/DO	PAD_GPIO_11	0	-	SDH_DAT1	SD Host Data 1
						1	-	SPI0_MOSI	SPI 0 Master Output, Slave Input
						2	-	SF2_D3	NOR FALSH controller signal2 Data 3
						3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG11	-
						8	-	-	-
						9	-	-	-
						10	-	-	-
						11	-	SWGPIO[11]	Software GPIO 11
						12	-	SDIO_DAT1	SDIO_DAT1
						16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
							reg_pwm1_io_sel=1	PWM0_CH1N	PWM0 Channel 1 Negative
						20	-	SPI1_MOSI	SPI 1 Master Output, Slave Input
						22	-	-	-
						23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select
						24	-	DISP_QSPI_SDA3	Display Quad SPI Serial Data 3
						25	-	-	-
						26	-	M0_JTAG_TDI	M0 JTAG Test Data Input
						27	-	PEC_11	PEC_11
						31	-	chip_clk_out[3]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
23	27	31		DI/DO	PAD_GPIO_12	0	-	-	-
						1	-	SPI0_SS	SPI 0 Slave Select
						2	-	-	-
						3	-	I2S_BCLK	I2S Bit Clock
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG0	-
						8	-	RMII_MDIO	RMII Management Data Input/Output
						9	-	CAM_DAT0	Camera Data 0
						10	-	ADC_CH8	ADC Channel 8
						11	-	SWGPIO[12]	Software GPIO 12
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
							reg_pwm1_io_sel=1	PWM0_CH2P	PWM0 Channel 2 Positive
						20	-	SPI1_SS	SPI 1 Slave Select
						22	-	DBI_TypeB_DB0	Display Bus Interface Type B Data Bit 0
						23	-	DBI_TypeC_SDA	Display Bus Interface Type C Serial Data
						24	-	DISP_QSPI_SCL	Display Quad SPI Serial Clock
						25	-	AUPWM_P	AUPWM_P
						26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
						27	-	PEC_12	PEC_12
						31	-	chip_clk_out[0]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
24	28	32		DI/DO	PAD_GPIO_13	0	-	-	-
						1	-	SPI0_SCLK	SPI 0 Serial Clock
						2	-	-	-
						3	-	I2S_FS	I2S Frame Sync
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG1	-
						8	-	RMII_MDC	RMII Management Data Clock
						9	-	CAM_DAT1	Camera Data 1
						10	-	ADC_CH9	ADC Channel 9
						11	-	SWGPIO[13]	Software GPIO 13
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
							reg_pwm1_io_sel=1	PWM0_CH2N	PWM0 Channel 2 Negative
						20	-	SPI1_SCLK	SPI 1 Serial Clock
						22	-	DBI_TypeB_DB1	Display Bus Interface Type B Data Bit 1
						23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control
						24	-	DISP_QSPI_CSn	Display Quad SPI Chip Select
						25	-	AUPWM_N	AUPWM_N
						26	-	M0_JTAG_TCK	M0 JTAG Test Clock
						27	-	PEC_13	PEC_13
						31	-	chip_clk_out[1]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	29	33		DI/DO	PAD_GPIO_14	0	-	-	-
						1	-	SPI0_MISO	SPI 0 Master Input, Slave Output
						2	-	-	-
						3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
						4	-	pdm_clk	PDM Clock Line
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG2	-
						8	-	RMII_TX_EN	RMII Transmit Enable
						9	-	CAM_DAT2	Camera Data 2
						10	-	-	-
						11	-	SWGPIO[14]	Software GPIO 14
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
							reg_pwm1_io_sel=1	PWM0_CH3P	PWM0 Channel 3 Positive
						20	-	SPI1_MISO	SPI 1 Master Input, Slave Output
						22	-	DBI_TypeB_DB2	Display Bus Interface Type B Data Bit 2
						23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock
						24	-	DISP_QSPI_SDA0	Display Quad SPI Serial Data 0
						25	-	-	-
						26	-	M0_JTAG_TDO	M0 JTAG Test Data Out
						27	-	PEC_14	PEC_14
						31	-	chip_clk_out[2]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	30	34		DI/DO	PAD_GPIO_15	0	-	-	-
						1	-	SPI0_MOSI	SPI 0 Master Output, Slave Input
						2	-	-	-
						3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
						4	-	pdm_in	PDM Data Line
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG3	-
						8	-	RMII_TXD[1]	RMII Transmit Data[1]
						9	-	CAM_DAT3	Camera Data 3
						10	-	-	-
						11	-	SWGPIO[15]	Software GPIO 15
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
							reg_pwm1_io_sel=1	PWM0_CH3N	PWM0 Channel 3 Negative
						20	-	SPI1_MOSI	SPI 1 Master Output, Slave Input
						22	-	DBI_TypeB_DB3	Display Bus Interface Type B Data Bit 3
						23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select
						24	-	DISP_QSPI_SDA1	Display Quad SPI Serial Data 1
						25	-	-	-
						26	-	M0_JTAG_TDI	M0 JTAG Test Data Input
						27	-	PEC_15	PEC_15
						31	-	chip_clk_out[3]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	-	35		DI/DO	PAD_GPIO_16	0	-	-	-
						1	-	SPI0_SS	SPI 0 Slave Select
						2	-	-	-
						3	-	I2S_BCLK	I2S Bit Clock
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG4	-
						8	-	RMII_TXD[0]	RMII Transmit Data[0]
						9	-	CAM_DAT4	Camera Data 4
						10	-	-	-
						11	-	SWGPIO[16]	Software GPIO 16
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
							reg_pwm1_io_sel=1	PWM0_CH0P	PWM0 Channel 0 Positive
						20	-	SPI1_SS	SPI 1 Slave Select
						22	-	DBI_TypeB_DB4	Display Bus Interface Type B Data Bit 4
						23	-	DBI_TypeC_SDA	Display Bus Interface Type C Serial Data
						24	-	DISP_QSPI_SDA2	Display Quad SPI Serial Data 2
						25	-	-	-
						26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
						27	-	PEC_16	PEC_16
						31	-	chip_clk_out[0]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	-	36		DI/DO	PAD_GPIO_17	0	-	-	-
						1	-	SPI0_SCLK	SPI 0 Serial Clock
						2	-	-	-
						3	-	I2S_FS	I2S Frame Sync
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG5	-
						8	-	RMII_REF_CLK	RMII Reference Clock
						9	-	CAM_DAT5	Camera Data 5
						10	-	-	-
						11	-	SWGPIO[17]	Software GPIO 17
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
							reg_pwm1_io_sel=1	PWM0_CH0N	PWM0 Channel 0 Negative
						20	-	SPI1_SCLK	SPI 1 Serial Clock
						22	-	DBI_TypeB_DB5	Display Bus Interface Type B Data Bit 5
						23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control
						24	-	DISP_QSPI_SDA3	Display Quad SPI Serial Data 3
						25	-	-	-
						26	-	M0_JTAG_TCK	M0 JTAG Test Clock
						27	-	PEC_17	PEC_17
						31	-	chip_clk_out[1]	Internal Clock Output of the Chip
25	31	37		Power,Input	VDD33IO	-	-	-	-
26	32	38		Power,Input	VDD18IO	-	-	-	-

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
27	33	39		Power,Input	PAD_GPIO_18	0	-	-	-
						1	-	SPI0_MISO	SPI 0 Master Input, Slave Output
						2	-	-	-
						3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG6	-
						8	-	RMII_RXD[1]	RMII Receive Data[1]
						9	-	CAM_DAT6	Camera Data 6
						10	-	-	-
						11	-	SWGPIO[18]	Software GPIO 18
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
							reg_pwm1_io_sel=1	PWM0_CH1P	PWM0 Channel 1 Positive
						20	-	SPI1_MISO	SPI 1 Master Input, Slave Output
						22	-	DBI_TypeB_DB6	Display Bus Interface Type B Data Bit 6
						23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock
						24	-	DISP_QSPI_SCL	Display Quad SPI Serial Clock
						25	-	AUPWM_P	AUPWM_P
						26	-	M0_JTAG_TDO	M0 JTAG Test Data Out
						27	-	PEC_18	PEC_18
						31	-	chip_clk_out[2]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
28	34	40		Power,Input	PAD_GPIO_19	0	-	-	-
						1	-	SPI0_MOSI	SPI 0 Master Output, Slave Input
						2	-	-	-
						3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG7	-
						8	-	RMII_RXD[0]	RMII Receive Data[0]
						9	-	CAM_DAT7	Camera Data 7
						10	-	-	-
						11	-	SWGPIO[19]	Software GPIO 19
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
							reg_pwm1_io_sel=1	PWM0_CH1N	PWM0 Channel 1 Negative
						20	-	SPI1_MOSI	SPI 1 Master Output, Slave Input
						22	-	DBI_TypeB_DB7	Display Bus Interface Type B Data Bit 7
						23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select
						24	-	DISP_QSPI_CSn	Display Quad SPI Chip Select
						25	-	AUPWM_N	AUPWM_N
						26	-	M0_JTAG_TDI	M0 JTAG Test Data Input
						27	-	PEC_19	PEC_19
						31	-	chip_clk_out[3]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
29	35	41		DI/DO	PAD_GPIO_20	0	-	-	-
						1	-	SPI0_SS	SPI 0 Slave Select
						2	-	-	-
						3	-	I2S_BCLK	I2S Bit Clock
						4	-	pdm_clk	PDM Clock Line
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG8	-
						8	-	RMII_RX_DV	RMII Receive Data Valid
						9	-	CAM_VSYNC	Camera Vertical Sync
						10	-	-	-
						11	-	SWGPIO[20]	Software GPIO 20
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
							reg_pwm1_io_sel=1	PWM0_CH2P	PWM0 Channel 2 Positive
						20	-	SPI1_SS	SPI 1 Slave Select
						22	-	-	-
						23	-	DBI_TypeC_SDA	Display Bus Interface Type C Serial Data
						24	-	DISP_QSPI_SDA0	Display Quad SPI Serial Data 0
						25	-	-	-
						26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
						27	-	PEC_20	PEC_20
						31	-	chip_clk_out[0]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
30	36	42		DI/DO	PAD_GPIO_21	0	-	-	-
						1	-	SPI0_SCLK	SPI 0 Serial Clock
						2	-	-	-
						3	-	I2S_FS	I2S Frame Sync
						4	-	pdm_in	PDM Data Line
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG9	-
						8	-	-	-
						9	-	CAM_CLK	Camera Clock
						10	-	-	-
						11	-	SWGPIO[21]	Software GPIO 21
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
							reg_pwm1_io_sel=1	PWM0_CH2N	PWM0 Channel 2 Negative
						20	-	SPI1_SCLK	SPI 1 Serial Clock
						22	-	-	-
						23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control
						24	-	DISP_QSPI_SDA1	Display Quad SPI Serial Data 1
						25	-	-	-
						26	-	M0_JTAG_TCK	M0 JTAG Test Clock
						27	-	PEC_21	PEC_21
						31	-	chip_clk_out[1]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
31	37	43		DI/DO	PAD_GPIO_22	0	-	-	-
						1	-	SPI0_MISO	SPI 0 Master Input, Slave Output
						2	-	-	-
						3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG10	-
						8	-	-	-
						9	-	CAM_HSYNC	Camera Horizontal Sync
						10	-	-	-
						11	-	SWGPIO[22]	Software GPIO 22
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
							reg_pwm1_io_sel=1	PWM0_CH3P	PWM0 Channel 3 Positive
						20	-	SPI1_MISO	SPI 1 Master Input, Slave Output
						22	-	-	-
						23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock
						24	-	DISP_QSPI_SDA2	Display Quad SPI Serial Data 2
						25	-	-	-
						26	-	M0_JTAG_TDO	M0 JTAG Test Data Out
						27	-	PEC_22	PEC_22
						31	-	chip_clk_out[2]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
32	38	44		DI/DO	PAD_GPIO_23	0	-	-	-
						1	-	SPI0_MOSI	SPI 0 Master Output, Slave Input
						2	-	-	-
						3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG11	-
						8	-	RMII_MDIO	RMII Management Data Input/Output
						9	-	CAM_VSYNC	Camera Vertical Sync
						10	-	-	-
						11	-	SWGPIO[23]	Software GPIO 23
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
							reg_pwm1_io_sel=1	PWM0_CH3N	PWM0 Channel 3 Negative
						20	-	SPI1_MOSI	SPI 1 Master Output, Slave Input
						22	-	-	-
						23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select
						24	-	DISP_QSPI_SDA3	Display Quad SPI Serial Data 3
						25	-	-	-
						26	-	M0_JTAG_TDI	M0 JTAG Test Data Input
						27	-	PEC_23	PEC_23
						31	-	chip_clk_out[3]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	39	45		DI/DO	PAD_GPIO_24	0	-	-	-
						1	-	SPI0_SS	SPI 0 Slave Select
						2	-	SF3_D3	NOR FALSH controller signal3 Data 3
						3	-	I2S_BCLK	I2S Bit Clock
						4	-	-	-
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG0	-
						8	-	RMII_MDC	RMII Management Data Clock
						9	-	CAM_DAT4	Camera Data 4
						10	-	-	-
						11	-	SWGPIO[24]	Software GPIO 24
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
							reg_pwm1_io_sel=1	PWM0_CH0P	PWM0 Channel 0 Positive
						20	-	SPI1_SS	SPI 1 Slave Select
						22	-	DBI_TypeB_DB0	Display Bus Interface Type B Data Bit 0
						23	-	DBI_TypeC_SDA	Display Bus Interface Type C Serial Data
						24	-	DISP_QSPI_SCL	Display Quad SPI Serial Clock
						25	-	AUPWM_P	AUPWM_P
						26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
						27	-	PEC_24	PEC_24
						31	-	chip_clk_out[0]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	40	46		DI/DO	PAD_GPIO_25	0	-	-	-
						1	-	SPI0_SCLK	SPI 0 Serial Clock
						2	-	SF3_CLK	NOR FALSH controller signal3 Clock
						3	-	I2S_FS	I2S Frame Sync
						4	-	-	-
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG1	-
						8	-	RMII_TX_EN	RMII Transmit Enable
						9	-	CAM_DAT5	Camera Data 5
						10	-	-	-
						11	-	SWGPIO[25]	Software GPIO 25
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
							reg_pwm1_io_sel=1	PWM0_CH0N	PWM0 Channel 0 Negative
						20	-	SPI1_SCLK	SPI 1 Serial Clock
						22	-	DBI_TypeB_DB1	Display Bus Interface Type B Data Bit 1
						23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control
						24	-	DISP_QSPI_CSn	Display Quad SPI Chip Select
						25	-	AUPWM_N	AUPWM_N
						26	-	M0_JTAG_TCK	M0 JTAG Test Clock
						27	-	PEC_25	PEC_25
						31	-	chip_clk_out[1]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	-	47		DI/DO	PAD_GPIO_26	0	-	-	-
						1	-	SPI0_MISO	SPI 0 Master Input, Slave Output
						2	-	SF3_D0	NOR FALSH controller signal3 Data 0
						3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
						4	-	pdm_clk	PDM Clock Line
						5	-	I2C_SCL_0	I2C 0 Serial Clock
						6	-	I2C_SCL_1	I2C 1 Serial Clock
						7	-	UART_SIG2	-
						8	-	RMII_TXD[1]	RMII Transmit Data[1]
						9	-	CAM_DAT0	Camera Data 0
						10	-	-	-
						11	-	SWGPIO[26]	Software GPIO 26
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
							reg_pwm1_io_sel=1	PWM0_CH1P	PWM0 Channel 1 Positive
						20	-	SPI1_MISO	SPI 1 Master Input, Slave Output
						22	-	DBI_TypeB_DB2	Display Bus Interface Type B Data Bit 2
						23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock
						24	-	DISP_QSPI_SDA0	Display Quad SPI Serial Data 0
						25	-	-	-
						26	-	M0_JTAG_TDO	M0 JTAG Test Data Out
						27	-	PEC_26	PEC_26
						31	-	chip_clk_out[2]	Internal Clock Output of the Chip

Table 3.1: Pin definition(continued)

QFN32	QFN40	QFN48	Voltage Domain	Type	Pin Name	GPIO Function	Signal Select	PAD Main	Description
-	-	48		DI/DO	PAD_GPIO_27	0	-	-	-
						1	-	SPI0_MOSI	SPI 0 Master Output, Slave Input
						2	-	SF3_D2	NOR FALSH controller signal3 Data 2
						3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
						4	-	pdm_in	PDM Data Line
						5	-	I2C_SDA_0	I2C 0 Serial Data
						6	-	I2C_SDA_1	I2C 1 Serial Data
						7	-	UART_SIG3	-
						8	-	RMII_TXD[0]	RMII Transmit Data[0]
						9	-	CAM_DAT1	Camera Data 1
						10	-	-	-
						11	-	SWGPIO[27]	Software GPIO 27
						12	-	-	-
						16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
							reg_pwm1_io_sel=1	PWM0_CH1N	PWM0 Channel 1 Negative
						20	-	SPI1_MOSI	SPI 1 Master Output, Slave Input
						22	-	DBI_TypeB_DB3	Display Bus Interface Type B Data Bit 3
						23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select
						24	-	DISP_QSPI_SDA1	Display Quad SPI Serial Data 1
						25	-	-	-
						26	-	M0_JTAG_TDI	M0 JTAG Test Data Input
						27	-	PEC_27	PEC_27
						31	-	chip_clk_out[3]	Internal Clock Output of the Chip

[1] UART SIGx(x=0-11) is used to select UART signal mapping. Taking UART_SIG0 and UART_SIG1 as examples, the following table shows the mapping relationship between UART_SIG0 and UART_SIG1.

[2] When selected as the SPI function, the default is SPI_MISO, which can be converted to SPI_MOSI through the register.

[3] SF1 is for in-pack flash,SF2 and SF3 cannot be used simultaneously.

Table 3.2: UART Signal Mapping

UART Signal	uart_sig_0_sel	Mapping Signal
UART_SIG0	uart_sig_0_sel=0	UART0_RTS
	uart_sig_0_sel=1	UART0_CTS
	uart_sig_0_sel=2	UART0_TXD
	uart_sig_0_sel=3	UART0_RXD
	uart_sig_0_sel=4	UART1_RTS
	uart_sig_0_sel=5	UART1_CTS
	uart_sig_0_sel=6	UART1_TXD
	uart_sig_0_sel=7	UART1_RXD
	uart_sig_0_sel=8	UART2_RTS
	uart_sig_0_sel=9	UART2_CTS
	uart_sig_0_sel=10	UART2_TXD
	uart_sig_0_sel=11	UART2_RXD
	uart_sig_1_sel=0	UART0_RTS

Table 3.2: UART Signal Mapping(continued)

UART Signal	uart_sig_0_sel	Mapping Signal
	uart_sig_1_sel=1	UART0_CTS
	uart_sig_1_sel=2	UART0_TXD
	uart_sig_1_sel=3	UART0_RXD
	uart_sig_1_sel=4	UART1_RTS
	uart_sig_1_sel=5	UART1_CTS
	uart_sig_1_sel=6	UART1_TXD
	uart_sig_1_sel=7	UART1_RXD
	uart_sig_1_sel=8	UART2_RTS
	uart_sig_1_sel=9	UART2_CTS
	uart_sig_1_sel=10	UART2_TXD
	uart_sig_1_sel=11	UART2_RXD

4 RF Characteristsic

5 Audio characteristic

6 Power Consumption

7 Electrical Specifications

7.1 Absolute Maximum Ratings

Table 7.1: Absolute Maximum Rating

Pin Name	Minimum	Maximum	Unit
VDD33PA, VDD33BAT, VDD33IO	-0.3	3.63	V
ESD Protection (HBM)		2000	V
Storage Temperature	-45	135	°C

7.2 Operating Condition

7.2.1 Power characteristics

Table 7.2: Recommended Power Operating Range

Pin Name	Minimum	Typical	Maximum	Unit
VDD33PA, VDD33BAT, VDD33IO	2.97	3.3	3.63	V

7.2.2 IO DC characteristics

Table 7.3: IO DC Characteristics

Sym-bol	Description	GPIO Number	Condition	Minimum	Typical	Maxi-mum	Unit
VOH	Output voltage high	GPIO 0-13, GPIO18-36	GPIO drive strength 0, source current = 5.4mA		0.9*VDDIO		V
			GPIO drive strength 0, source current = 12.2mA				
			GPIO drive strength 0, source current = 14.9mA				
			GPIO drive strength 0, source current = 21.6mA				

Table 7.3: IO DC Characteristics(continued)

Sym-bol	Description	GPIO Number	Condition	Minimum	Typical	Maxi-mum	Unit
		GPIO 14-17	GPIO drive strength 0, source current = 6.3mA				
			GPIO drive strength 0, source current = 12.6mA				
			GPIO drive strength 0, source current = 18.8mA				
			GPIO drive strength 0, source current = 25.1mA				
VOL	Output voltage low	GPIO 0-13, GPIO18-36	GPIO drive strength 0, sink current = 9.3mA		0.1*VDDIO		V
			GPIO drive strength 0, sink current = 18.5mA				
			GPIO drive strength 0, sink current = 23.2mA				
			GPIO drive strength 0, sink current = 32.4mA				
		GPIO 14-17	GPIO drive strength 0, sink current = 5.8mA				
			GPIO drive strength 0, sink current = 11.6mA				
			GPIO drive strength 0, sink current = 17.4mA				
			GPIO drive strength 0, sink current = 23.2mA				
VIH	Input voltage high			2			V
VIL	Input voltage low					0.8	V

7.2.3 Power-On Sequence

To ensure normal power-on startup, the power supply, reset, and Bootstrap pins must meet the corresponding timing requirements.

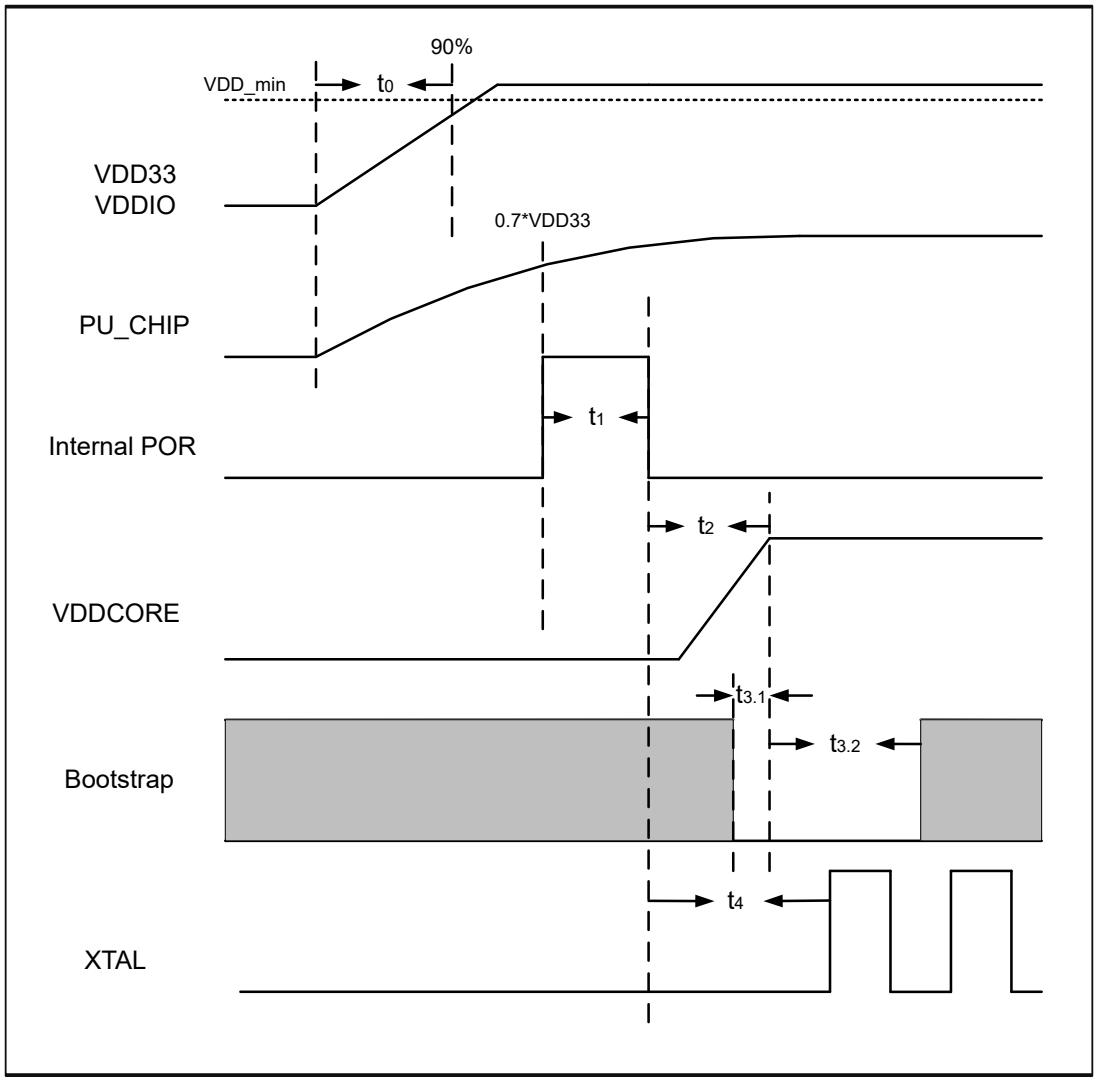


Fig. 7.1: Power-On Sequence

Table 7.4: Power-On Sequence Parameter Description

Parameter	Description	Minimum(ms)	Typical(ms)	Maximum(ms)
t_0	Power supply voltage rise time to 90% [1]		0.1	
t_1	Internal POR duration		2.5	
t_2	Time from POR going low to VDDCORE output		2	
$t_{3.1}$	Preparation time for Bootstrap pin [2]before VDD-CORE is established	0		
$t_{3.2}$	Time for Bootstrap pin to maintain valid level	2		
t_4	Time from POR going low to XTAL oscillation		3	

[1] VDD_min is the minimum value to ensure the chip operates normally.

[2] The Bootstrap pin is GPIO36.

7.2.4 Shutdown Sequence

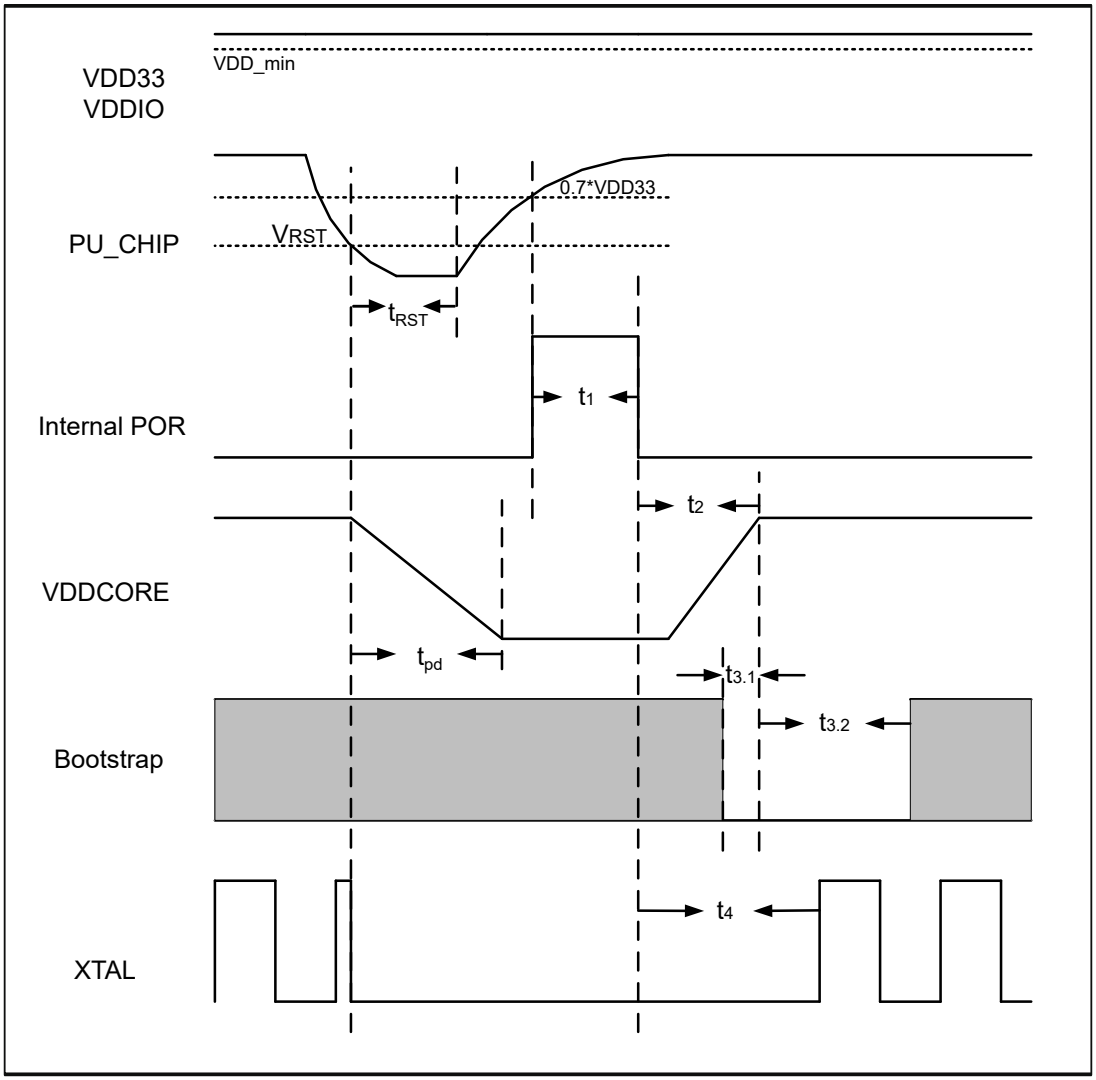


Fig. 7.2: Shutdown Sequence

Table 7.5: Shutdown sequence parameters

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{RST}	PU_CHIP will shut down only when below this value	0	0.1*VDD33	0.3*VDD33	V
t_{RST}	Time for PU_CHIP to drop below VRST	1	1		ms
t_{pd}	Time for VDDCORE to drop to 0 after shutdown	1	1		ms

7.2.5 Temperature sensor characteristics

Table 7.6: Temperature Sensor Characteristics

Item		Minimum	Typical	Maximum	Unit
Ta	Ambient temperature of the main chip	-40		105	°C
	Ambient temperature of the multi-chip package	-40		85	°C
Tj	Junction temperature	-40		125	°C

7.2.6 General operating conditions

Table 7.7: General Operating Conditions

Item	Description	Minimum	Typical	Maximum	Unit
FCPU	CPU/TCM/Cache clock frequency		320		MHz
FBUS	System bus clock frequency		80		MHz

7.2.7 GPADC characteristics

Table 7.8: GPADC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
VDDA	VDD supply			3.3	3.6	V
T	Working temperature		-40		125	°C
I	Current consumption of ADC on VDD 18	PGA off (2M clock)		80		μA
		PGA on (2M clock)		150		
Fclk	ADC input top clock frequency	Clock from SOC			2	MHz
Fsample	Sampling rate		0.05		2	MHz
Vin	Input conversion voltage range	Differential mode			6.4	V(vpp)
		Single-ended mode	0.02		3.2	
Rin	Total input channel resistance	Without PGA With PGA			10 >1000	KΩ
Tpu	Power up time				2	uS

Table 7.8: GPADC Characteristics(continued)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Tconv	Total conversion time	12bit mode			1	1/Fsample
		14bit mode [1]			16	
		14bit mode [2]			64	
		16bit mode [3]			128	
		16bit mode [4]			256	

[1] res_sel=1

[2] res_sel=2

[3] res_sel=3

[4] res_sel=4

Table 7.9: ADC electrical characteristic

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
DNL	Differential linearity error				+/-1	LSB
INL	Integral linearity error				+/-1.5	LSB
Total error	DC measure Total error				+/-10mV	max
ENOB	Effective number of bits	12bit mode (50KHz input)	10	9.7		bit
		14bit mode (2.5KHz input)	10.8	11.4		
		16bit mode (1KHz input)	11.6	12.3		
SNDR	Signal-to-noise-distortion (PGA off)	12bit mode (50KHz input)	62	60		dB
		14bit mode (2.5KHz input)	66.5	72.4		
		16bit mode (1KHz input)	71.6	76.8		
SNR	Signal-to-noise-distortion (PGA off)	12bit mode (50KHz input)	62.5	65.6		dB
		14bit mode (2.5KHz input)	68	71		
		16bit mode (1KHz input)	72	77.8		
SNDR	Signal-to-noise-distortion (PGA gain=1)	12bit mode (50KHz input)	61	64		dB
		14bit mode (2.5KHz input)	65.5	69.5		
		16bit mode (1KHz input)	72	74		

8 Product use

8.1 Moisture Sensitivity Level(MSL)

The moisture sensitivity level of the chip is: MSL3. After the vacuum package is opened, it needs to be used up within 168 hours (7 days) at ≤30°C/60%RH, otherwise it needs to be baked and put online.

For baking temperature and time, please refer to IPC/JEDECJ-STD-033B01.

Table 8.1: Reference Conditions for Drying Mounted or Unmounted SMD Packages (User Bake: Floor life begins counting at time = 0 after bake)

Package Body	Level	Bake @ 125°C		Bake @ 90°C ≤5% RH		Bake @ 40°C ≤5% RH	
		Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h
Thickness ≤1.4 mm	2	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	2a	7 hours	5 hours	23 hours	13 hours	9 days	7 days
	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days

8.2 Electro-Static discharge（ESD）

- Human Body Model(HBM): 2000V
- Charged-Device Model(CDM): 500V

8.3 Reflow Profile

For details, please refer to IPC/JEDEC J-STD-020E.

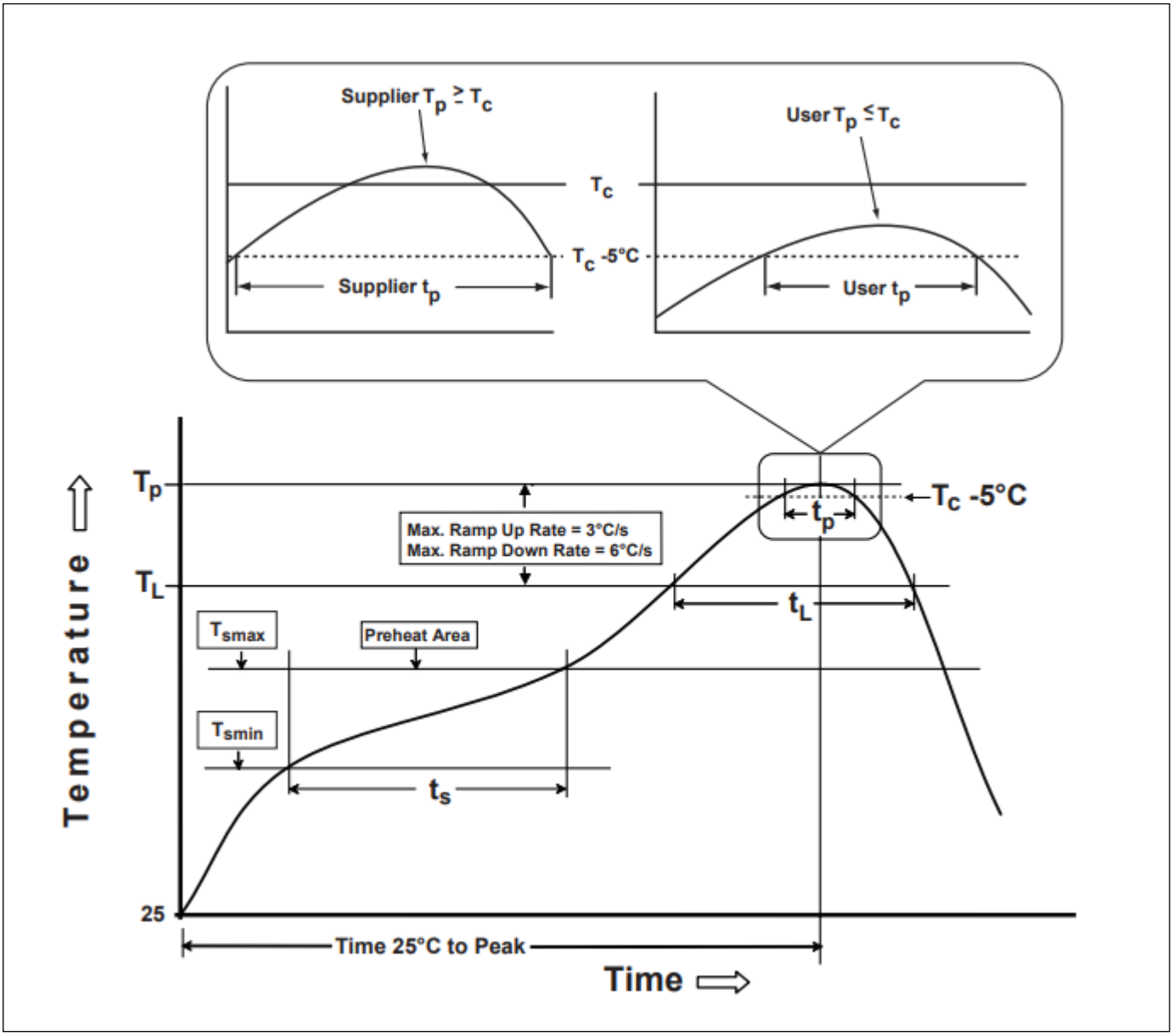


Fig. 8.1: Classification Profile (Not to scale)

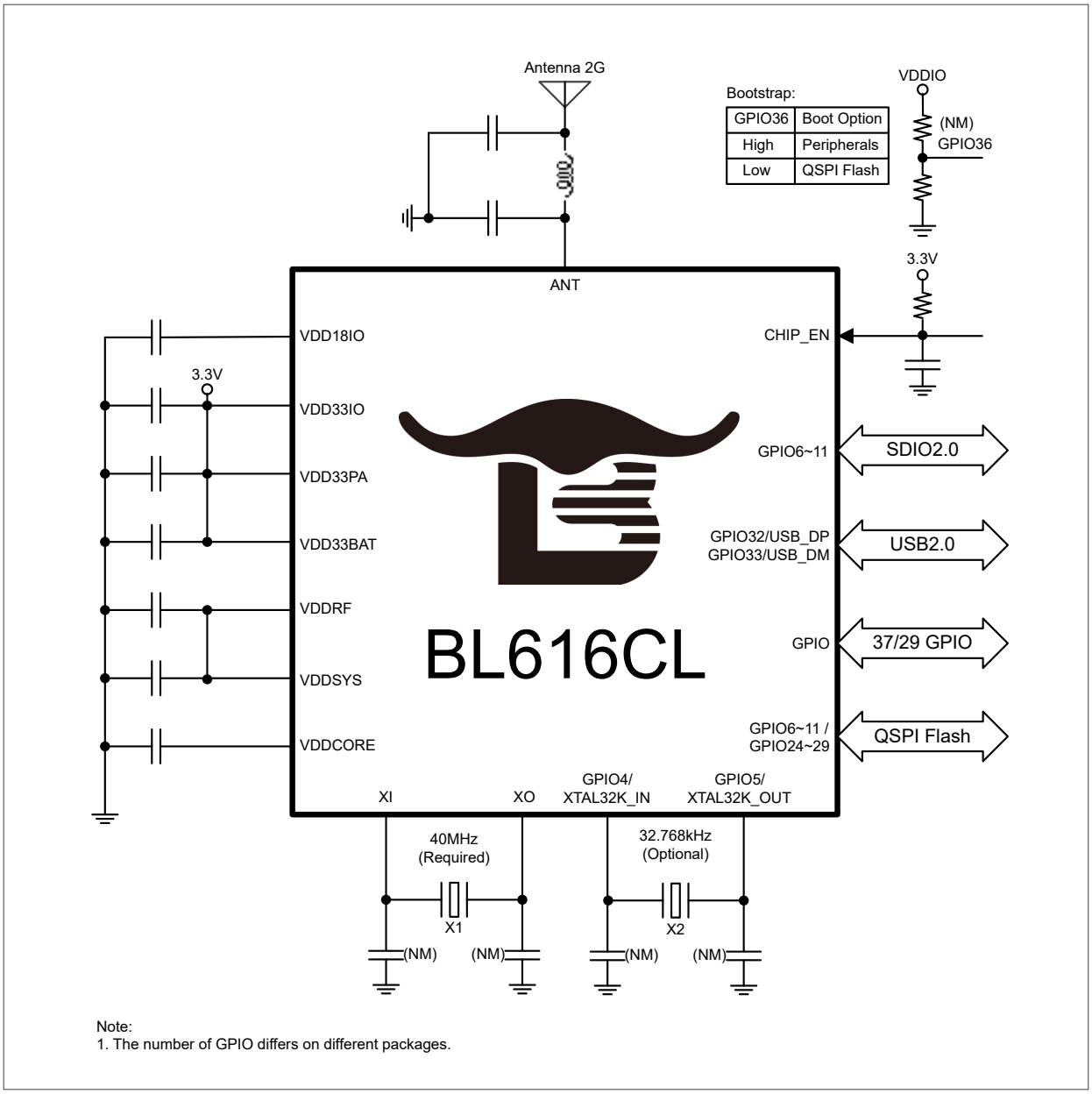
Table 8.2: Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.

Table 8.2: Classification Reflow Profiles(continued)

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	240 °C+0/-5 °C	250 °C+0/-5 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c)	10-30 seconds	20-40 seconds
Ramp-down rate ($T_p$to T_L)	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max
- Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.		

9 Reference Design



Note:
1. The number of GPIO differs on different packages.

Fig. 9.1: BL616CL Reference Design

10 Package Information(QFN32)

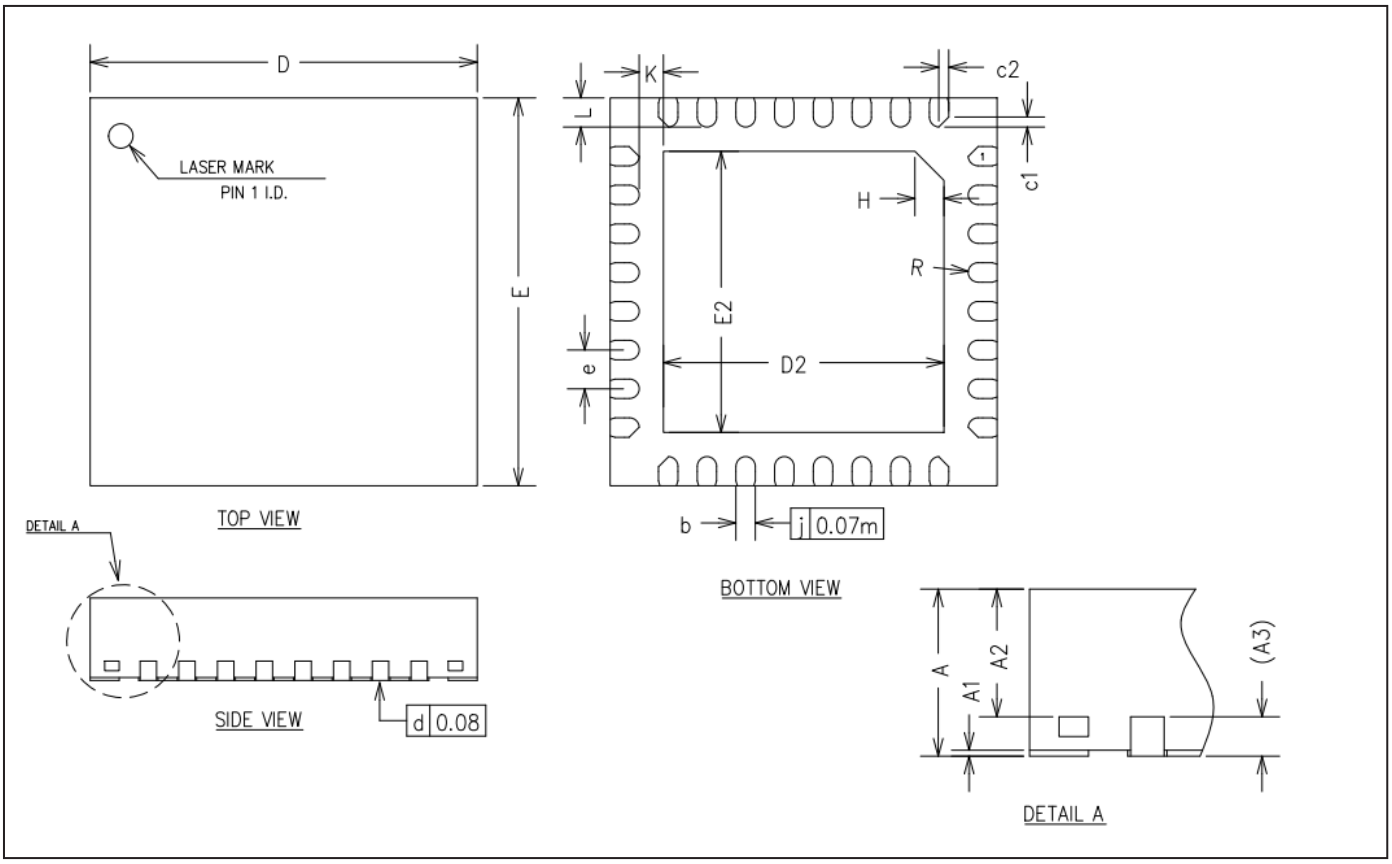


Fig. 10.1: QFN32 Package drawing

Table 10.1: QFN32 Size Description

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00

Table 10.1: QFN32 Size Description(continued)

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30REF		
K	0.25REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

11 Package Information(QFN40)

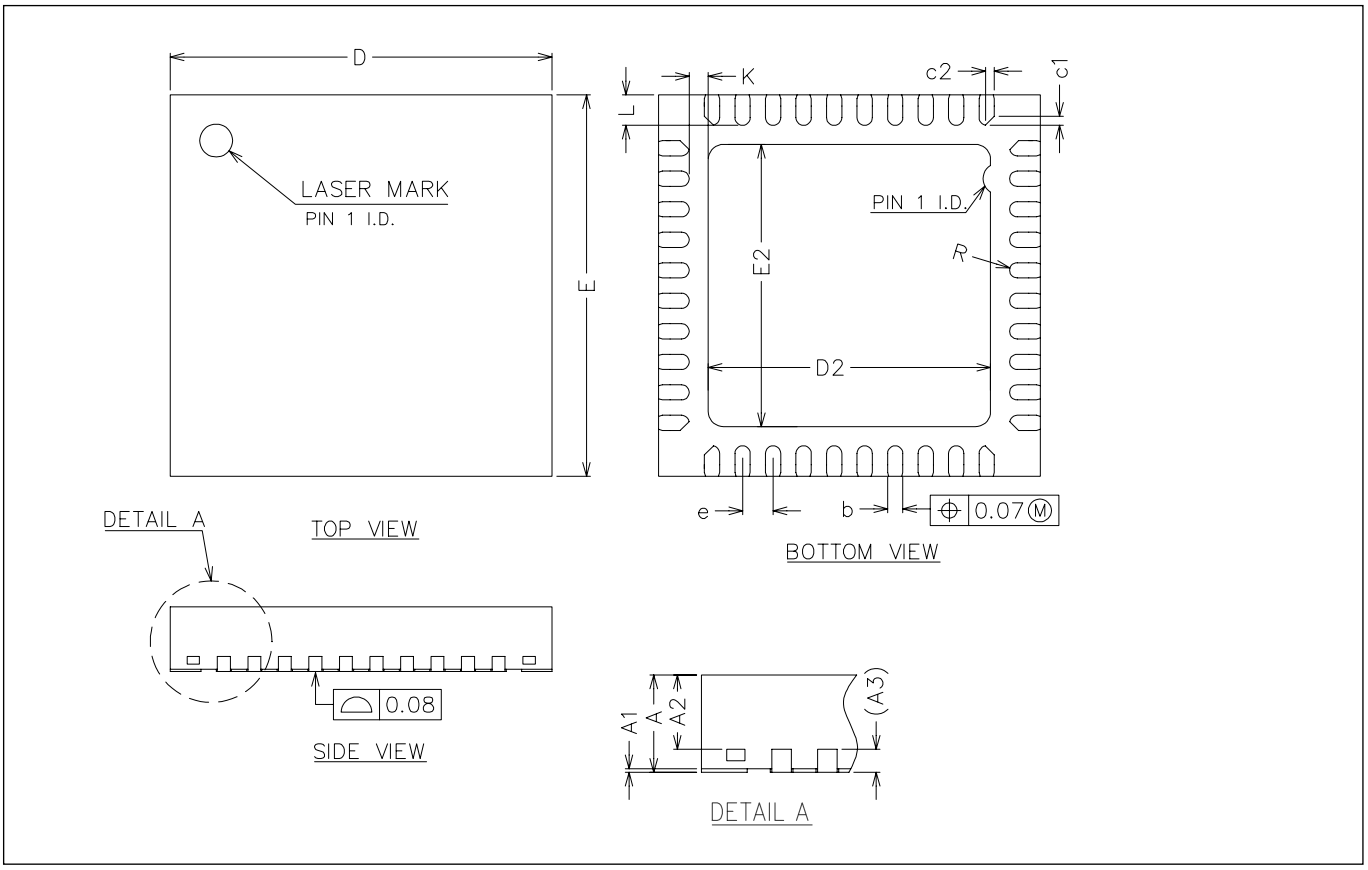


Fig. 11.1: QFN40 Package drawing

Table 11.1: QFN40 Size Description

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3	0.20 REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80

Table 11.1: QFN40 Size Description(continued)

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
c1	-	0.12	-
c2	-	0.12	-

12 Package Information(QFN48)

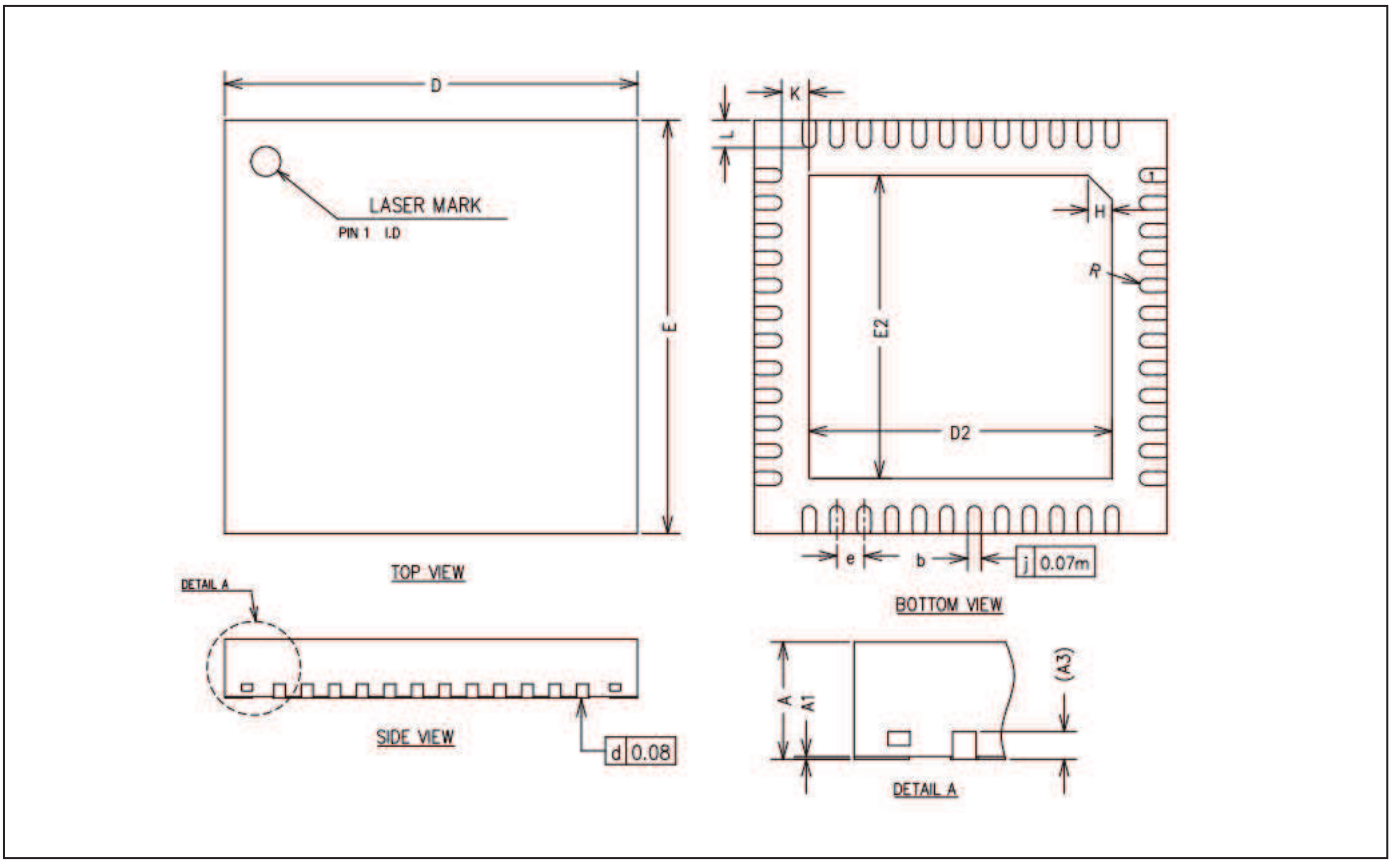


Fig. 12.1: QFN48 Package drawing

Table 12.1: QFN48 Size Description

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A3	0.20REF		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.30	4.40	4.50
E2	4.30	4.40	4.50

Table 12.1: QFN48 Size Description(continued)

SYMBOL	UNIT OF MEASURE = MILLIMETER		
	MIN	NOM	MAX
e	0.30	0.40	0.50
H	0.35REF		
K	0.30	0.40	0.50
L	0.30	0.40	0.50
R	0.075	-	-

13 Top Marking Definition

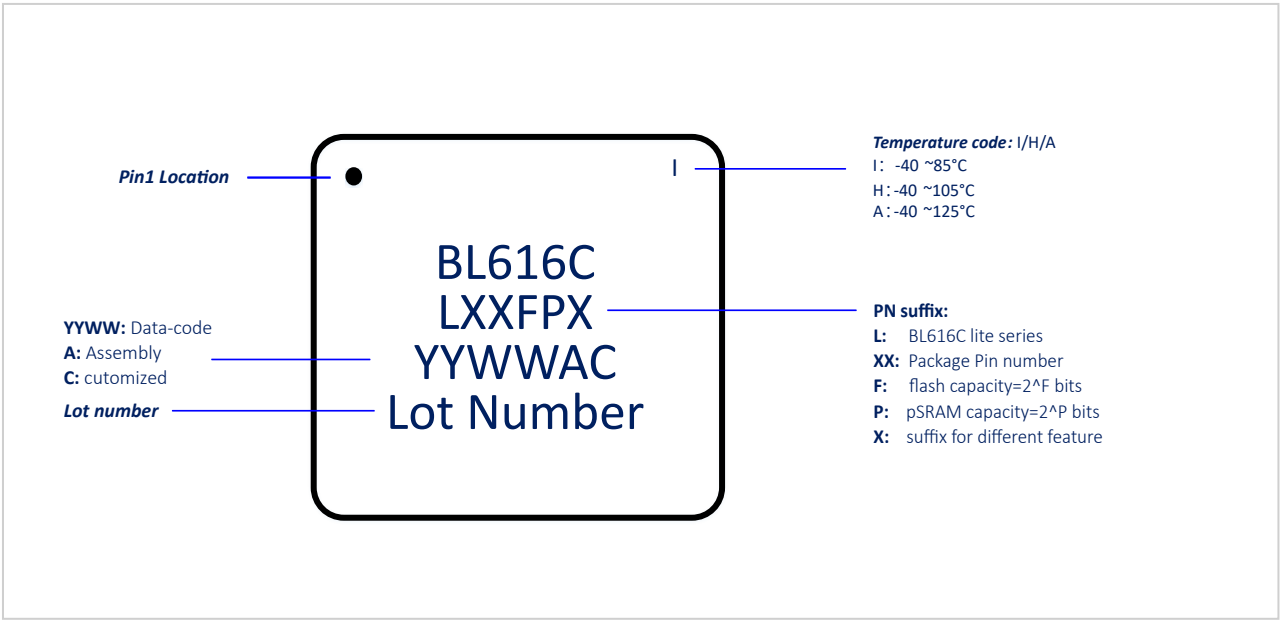


Fig. 13.1: BL616CL series marking information

14 Ordering Information

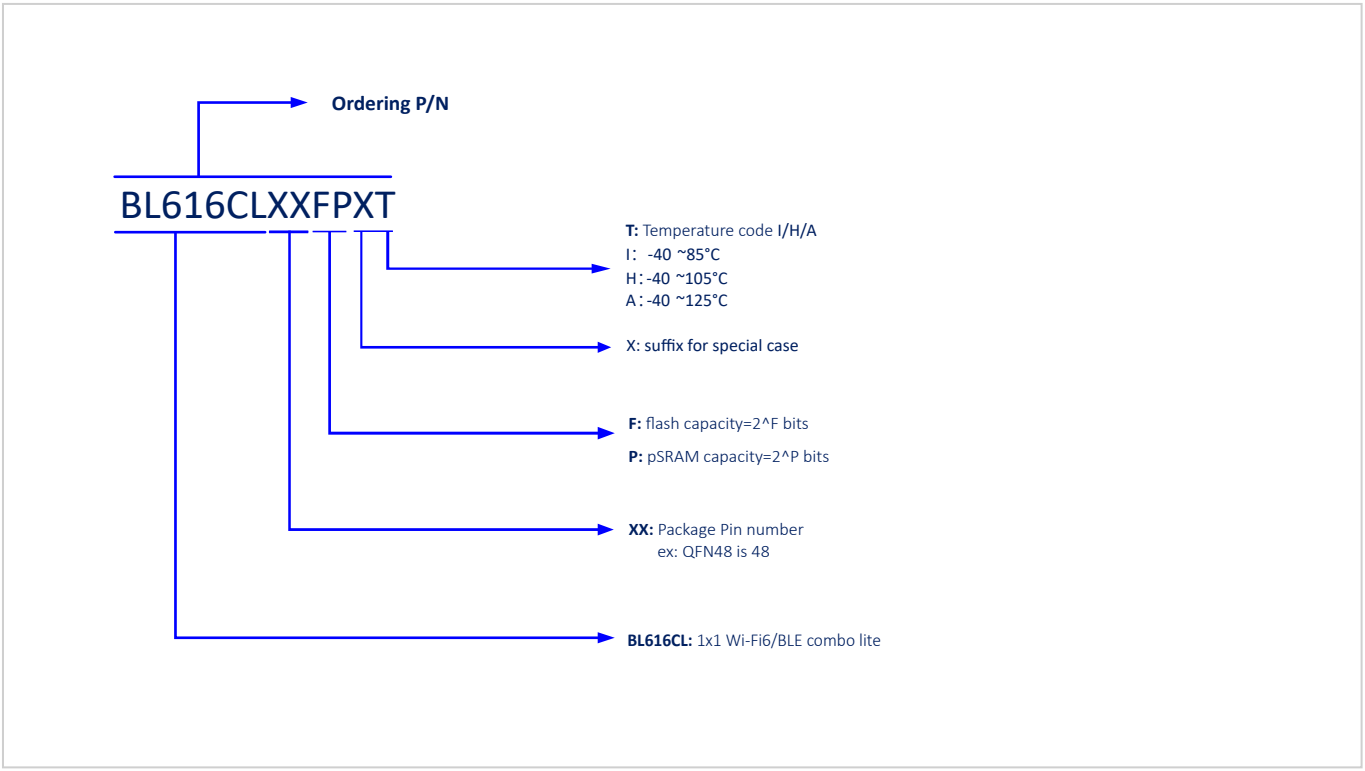


Fig. 14.1: Part Number

Note: The chip ordering part number rules are illustrated above. For specific part number information, please contact support personnel.

Table 14.1: Product Packing Information

Package Size(mm)	Reel size	Quantity per Master Carton	Quantity per Roll	Reel Diameter	Tape Width	Tape Pitch	Moisture Sensitivity Level	Package Type
QFN 4*4	13”	30000	6000	330mm	12mm	8mm	MSL3	Tape reel
QFN 6*6	13”	15000	3000	330mm	16mm	12mm	MSL3	

15 Revision history

Table 15.1: Document revision history

Date	Revision	Changes
2024/12/17	0.9	Initial release
2025/8/14	0.9.1	Add QFN32 package information
2025/9/17	0.9.2	Fix some typos
2026/3/7	0.9.3	Add ordering information
2026/3/20	0.9.4	Update QFN32 package information